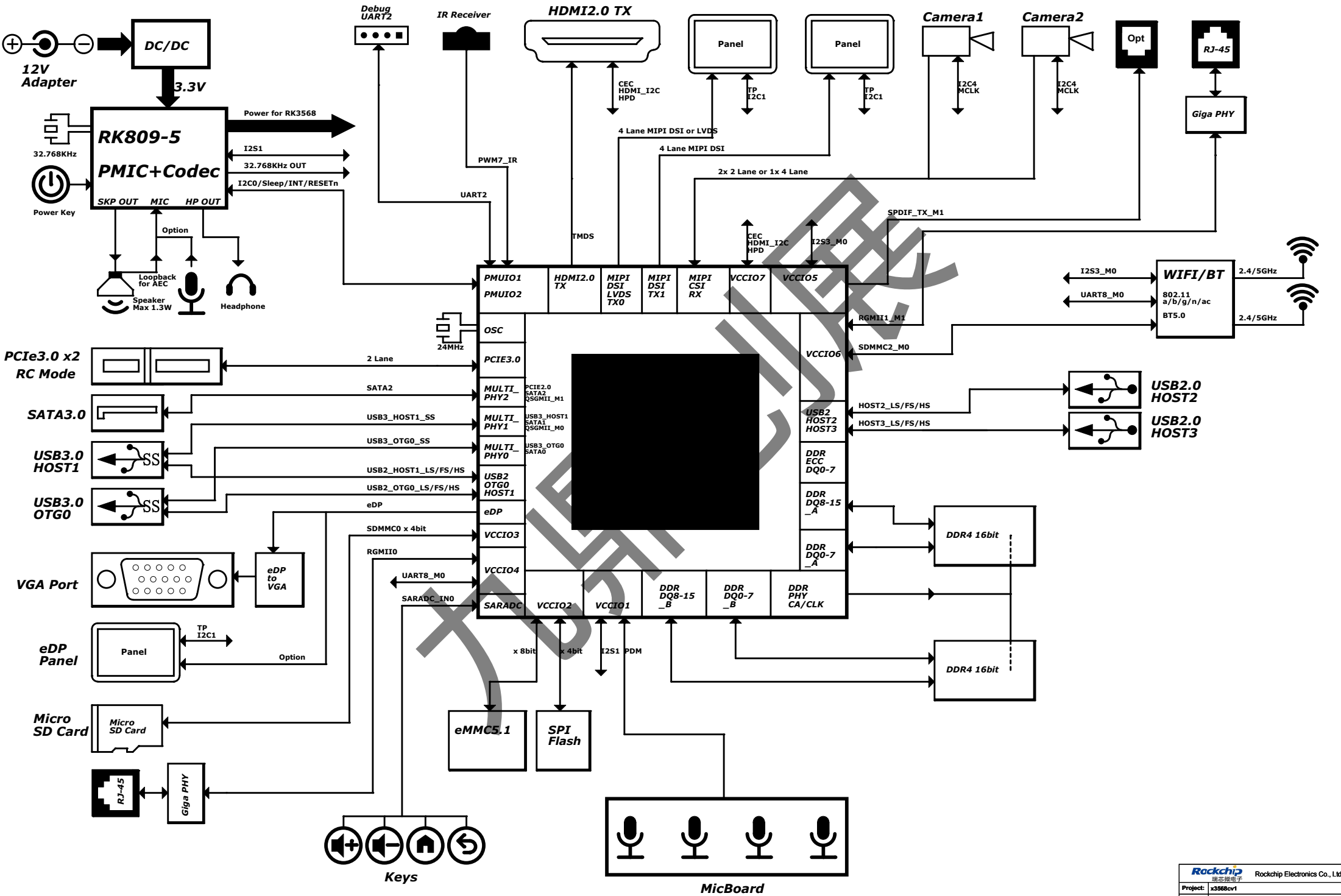
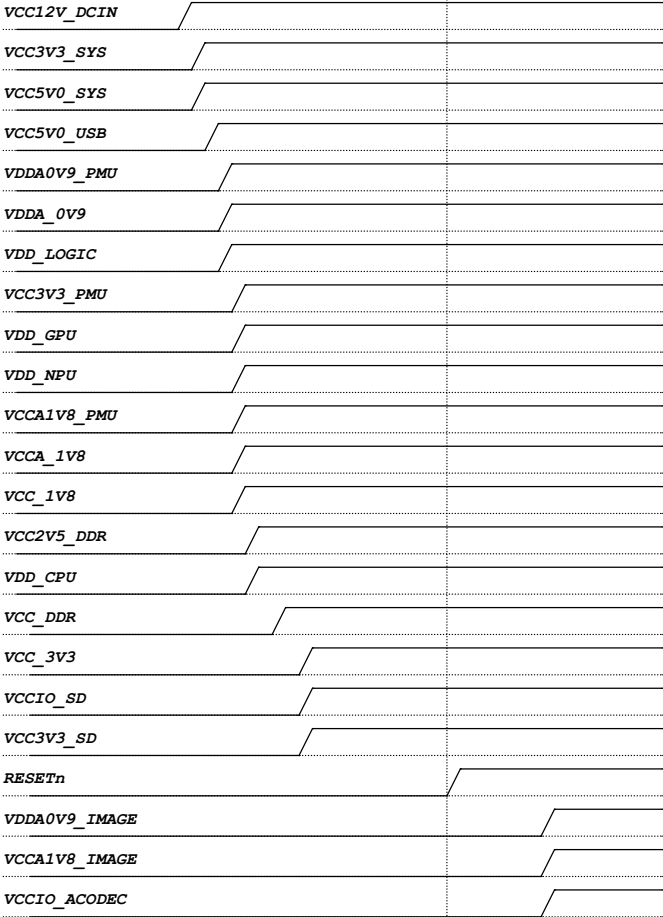


RK3568 Ref Block Diagram



Power Sequence

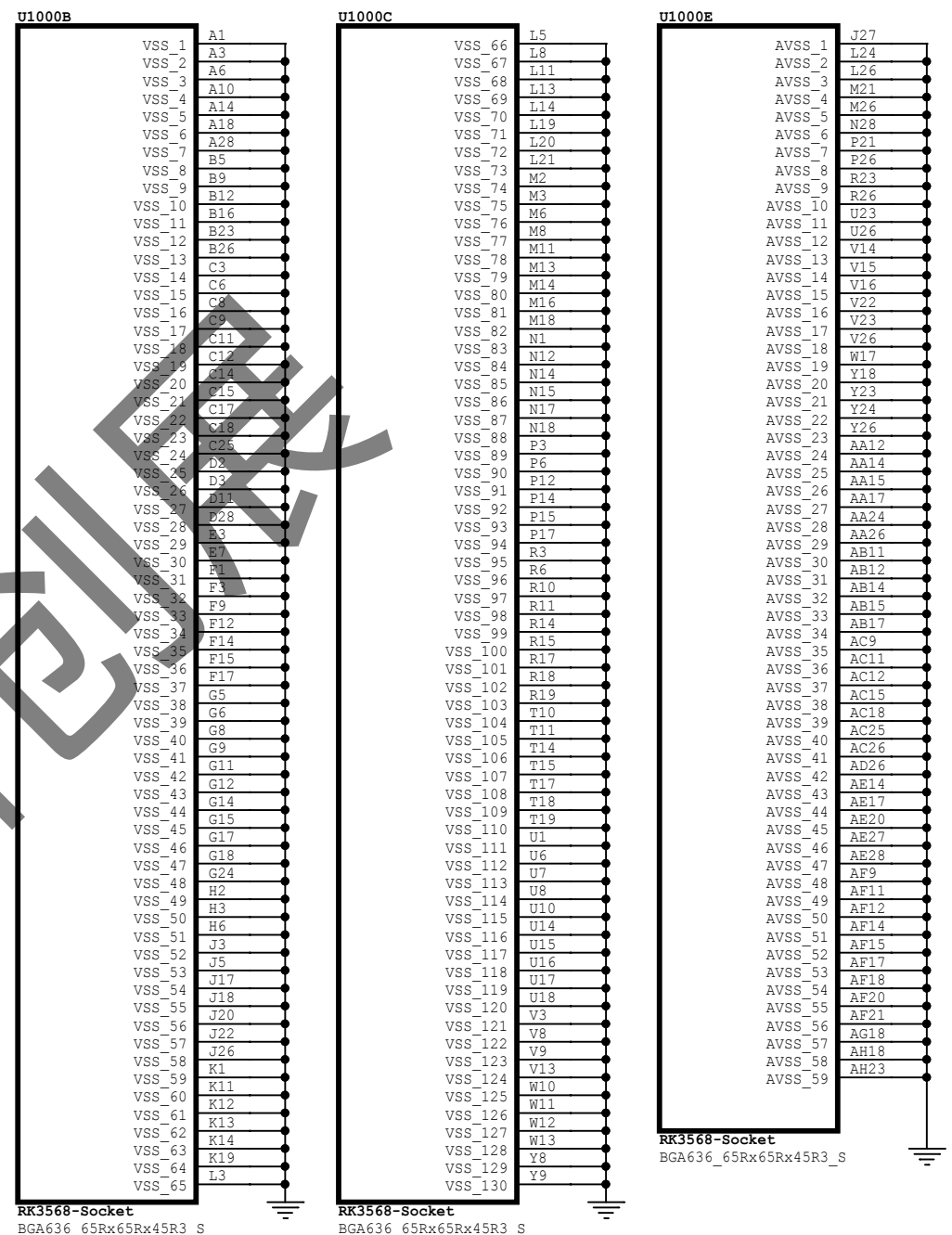
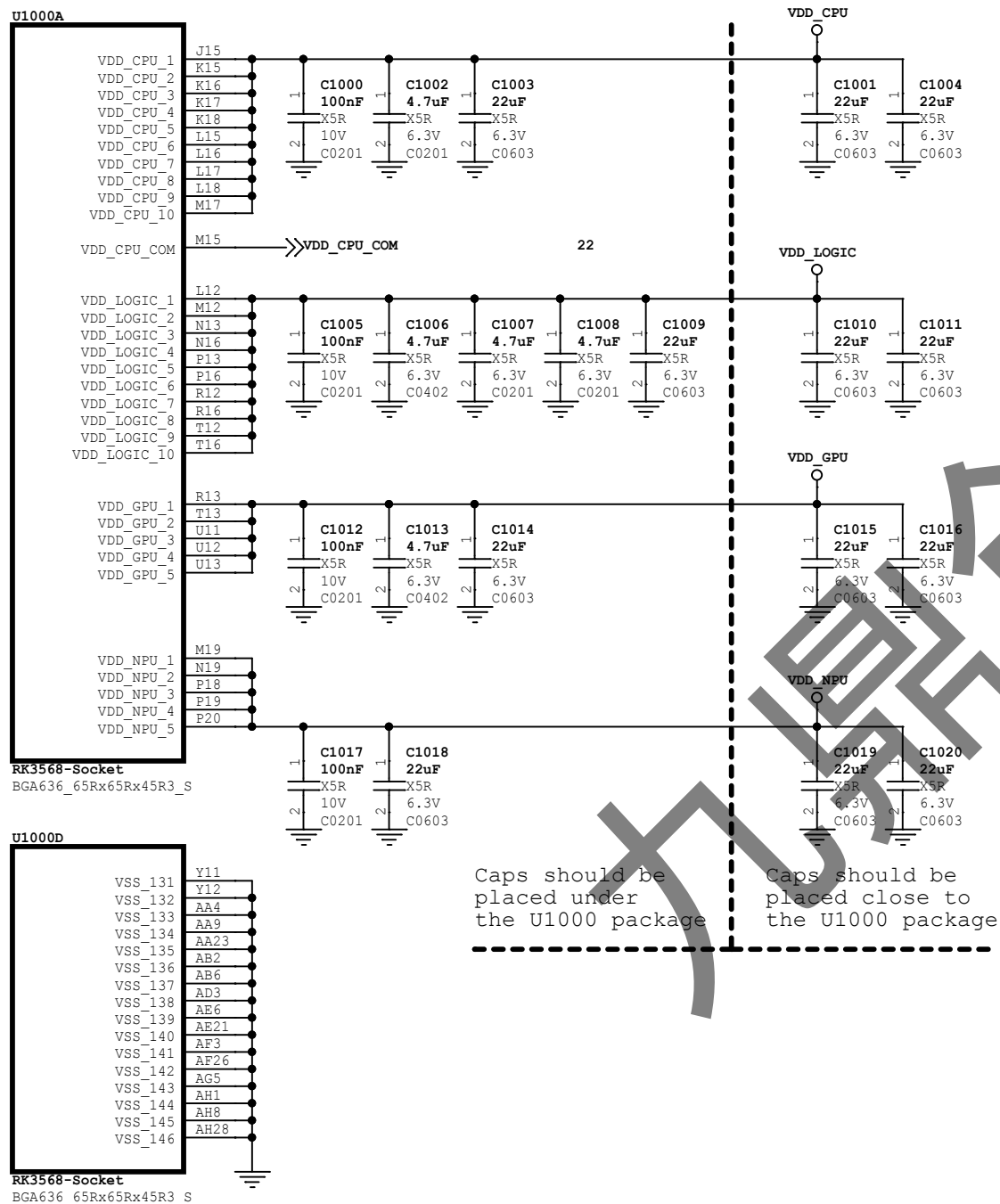


Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETh			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	OFF	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	ON	TBD	TBD

IO Power Domain Map
Updates must be Revision accordingly!

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

RK3568 ABCDE (Power&Gnd)



Rockchip
瑞芯微电子

Rockchip Electronics Co., Ltd

Project:	x3568cv1
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File:	03.RK3568_Power/GND
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Date:	Monday, August 29, 2022
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Rev:	V1.0
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Designed by:	Zhangda
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Reviewed by:

Default	Sheet:	3 of 17
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Rockchip Confidential

RK3568_F (DDR PHY)

U1000F

DDR4_DQ0_A	DDR DQ0 A	F2
DDR4_DQ1_A	DDR DQ1 A	E1
DDR4_DQ2_A	DDR DQ2 A	E2
DDR4_DQ3_A	DDR DQ3 A	D1
DDR4_DQ4_A	DDR DQ4 A	J1
DDR4_DQ5_A	DDR DQ5 A	J2
DDR4_DQ6_A	DDR DQ6 A	H1
DDR4_DQ7_A	DDR DQ7 A	H4
DDR4_DQ8_A	DDR DQ8 A	M1
DDR4_DQ9_A	DDR DQ9 A	M2
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DDR4_DQ11_A	DDR DQ11 A	L6
DDR4_DQ12_A	DDR DQ12 A	R2
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DDR4_DQ328_A	DDR DQ328 A	E325
DDR4_DQ329_A	DDR DQ329 A	E326
DDR4_DQ330_A	DDR DQ330 A	E327
DDR4_DQ331_A	DDR DQ331 A	

Diagram illustrating the power and signal connections for the RK3568_G (OSC/PLL/PMUIO1/2) module, showing the U1000G package and its connections to various power domains and logic power.

OSC (Oscillator) Section:

- Y1200: 24MHz, 12pF
- C1201: 15pF
- C0201: 50V
- R1200: 1, 2, 22R, 5%
- R0201: 5%
- XOUT24M: AF27
- XIN24M: AF28
- Operating Voltage = 1.8V (PMUPLL_AVDD_1V8)

PMU PLL (PMU PLL) Section:

- V21: PMUPLL_AVDD_0V9
- V21: PMUPLL_AVDD_1V8
- V20: PMUPLL_AVSS
- C1204: 1uF
- C1205: 100nF
- C0402: 10V
- C0201: 10V
- C1206: 1uF
- C1207: 100nF
- C0402: 10V
- C0201: 10V
- V20: PMUPLL_AVSS

SYS PLL (System PLL) Section:

- F11: SYSPLL_AVDD_0V9
- N10: SYSPLL_AVDD_1V8
- N11: SYSPLL_AVSS
- C1208: 1uF
- C1209: 100nF
- C0402: 10V
- C0201: 10V
- C1211: 1uF
- C1212: 100nF
- C0402: 10V
- C0201: 10V

PMUIO1 Domain:

- Operating Voltage=3.3V Only
- REFCLK_OUT / GPIO0_A0_d
- TSADC_SHUT_M0 / GPIO0_A1_d
- PMIC_SLEEP / GPIO0_A2_d
- SDMMC0_DET / SATA_CP_DET / PCIE30X1_CLKREQ_M0 / GPIO0_A3_d
- SDMMC0_PAREN / SATA_MP_SWITCH / PCIE20_CLKREQ_M0 / GPIO0_A4_d
- GPU_PWREN / SATA_CP_POD / PCIE30X2_CLKREQ_M0 / GPIO0_A5_d
- FLASH_VOL_SEL / GPIO0_A6_d

PMUIO2 Domain:

- Operating Voltage=1.8V/3.3V
- CLK32K_IN / CLK32K_OUT0 / PCIE30X2_BUTTONRSTn / GPIO0_B0_d
- I2C0_SCL / GPIO0_B1_d
- I2C0_SDA / GPIO0_B2_d
- I2C1_SCL / CAN0_RX_M0 / PCIE30X1_BUTTONRSTn / MCU_STAT_T00 / GPIO0_B3_d
- I2C1_SDA / CAN0_RX_M0 / PCIE20_BUTTONRSTn / MCU_STAT_T00 / GPIO0_B4_d
- I2C2_SCL_M0 / SPI0_CLK_M0 / PCIE20_WAREn_M0 / PWM1_M1 / GPIO0_B5_d
- I2C2_SDA_M0 / SPI0_M0ST_M0 / PCIE20_P0RSTn_M0 / PWM2_M1 / GPIO0_B6_d
- PMU0_M0 / CPU0VTS / GPIO0_B7_d
- PWM1_M0 / GPU0VTS / UART0_RX / GPIO0_C0_d
- PWM2_M0 / GPU0VTS / UART0_TX / GPIO0_C1_d
- PWM3_IR / EDP_HPDIN_M1 / PCIE30X1_WAREn_M0 / MCU_STAT_T00 / GPIO0_C2_d
- PWM4 / VOP_PWM_M0 / PCIE30X1_P0RSTn_M0 / MCU_STAT_T00 / GPIO0_C3_d
- PWM5 / SPI0_CS0_M0 / PCIE30X2_WAREn_M0 / GPIO0_C4_d
- PWM6 / SPI0_CS0_M0 / PCIE30X2_P0RSTn_M0 / GPIO0_C5_d
- PWM7_IR / SPI0_CS0_M0 / PCIE30X2_P0RSTn_M0 / GPIO0_C6_d
- HDMI_TX_CEC_M1 / PWM0_M1 / UART0_TX / GPIO0_C7_d
- UART2_RX_M0 / GPIO0_D0_d
- UART2_TX_M0 / GPIO0_D1_d

PMUIO1/2/OSC Domain Logic Power:

- Operating Voltage=0.9V
- PMU_VDD_LOGIC_0V9

Other Connections:

- TSADC_SHUT_M0
- REFCLK_OUT_CAM
- PMIC_SLEEP_H
- PMIC_INT_L
- SDMMC0_DET_L
- GPIO0_A5
- GPIO0_A6
- GPIO0_A7
- VCC3V3_PMU
- R1207: 2.2K
- R1208: 2.2K
- I2C0_SCL_PMIC
- I2C0_SDA_PMIC
- I2C0_SCL_PMIC
- I2C0_SDA_PMIC
- I2C1_SCL_TP
- I2C1_SDA_TP
- TP_INT_L_GPIO0_B5
- TP_RST_L_GPIO0_B6
- GPIO0_C3
- GPIO0_C6
- PWM7_IR
- UART2_RX_M0_DEBUG
- UART2_TX_M0_DEBUG
- VCC3V3_PMU
- C1210: 100nF
- X5R: 10V
- C0201: 10V
- VDDA0V9_PMU
- C1213: 100nF
- C1214: 1uF
- X5R: 10V
- C0402: 10V

Note:

- Caps of between dashed green lines and U1000 should be placed under the U1000 package.
- Other caps should be placed close to the U1000 package.

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Project: x3568cv1

File: 05.RK3568_OSC/PLL/PMUIO

Date: Monday, August 26, 2022

Designed by: Zhangdz

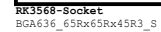
Reviewed by: Default

Rev: V1.0

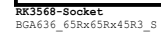
Sheet: 5 of 17

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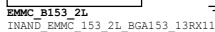
U1000I



U1000J



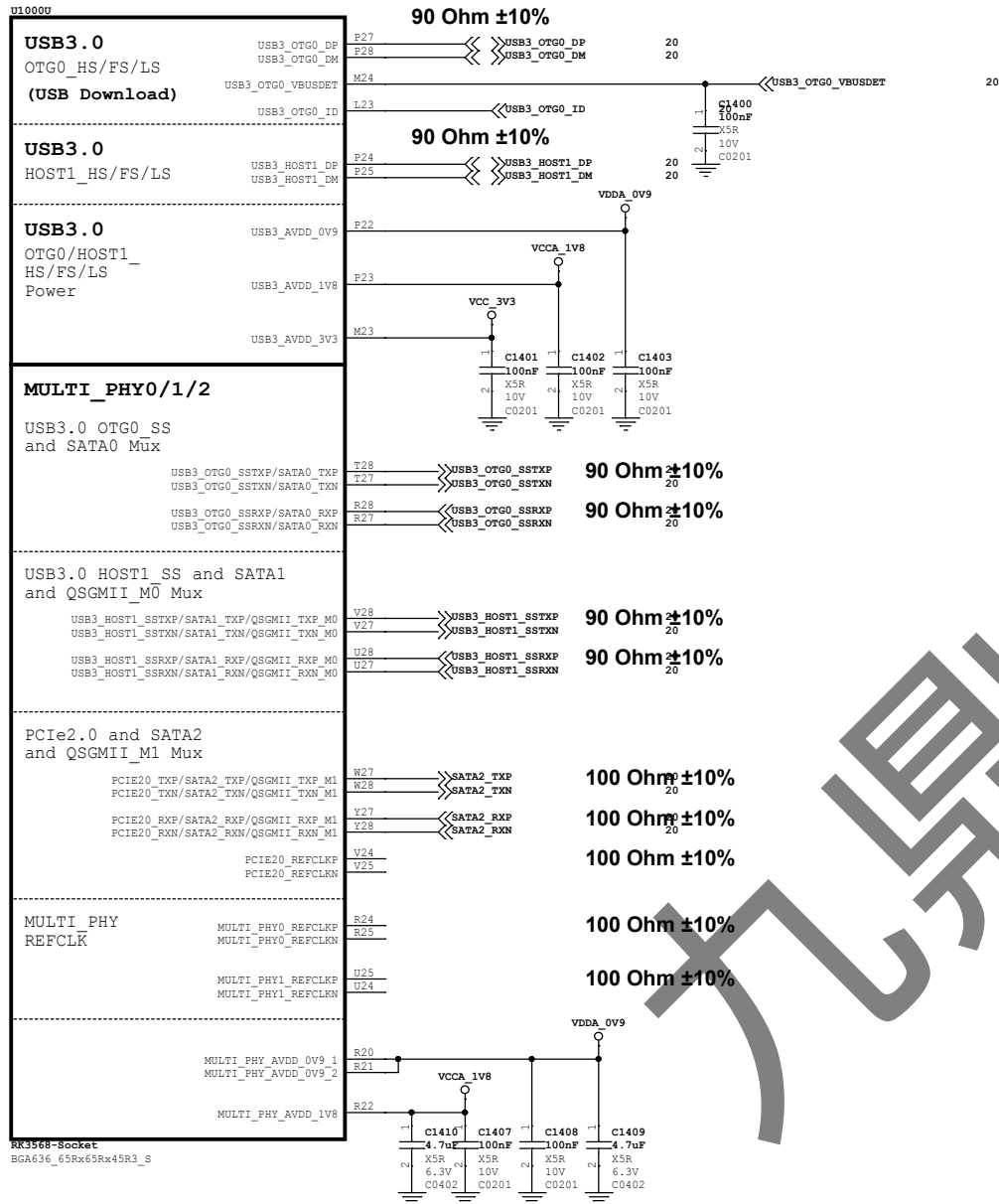
Caps of between dashed green lines and U1000
should be placed under the U1000 package



Rockchip
瑞芯微电子

Project:	x3568cv1				
File:	06.RK3568_Flash/SD Controller				
Date:	Saturday, December 17, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	6 of 17

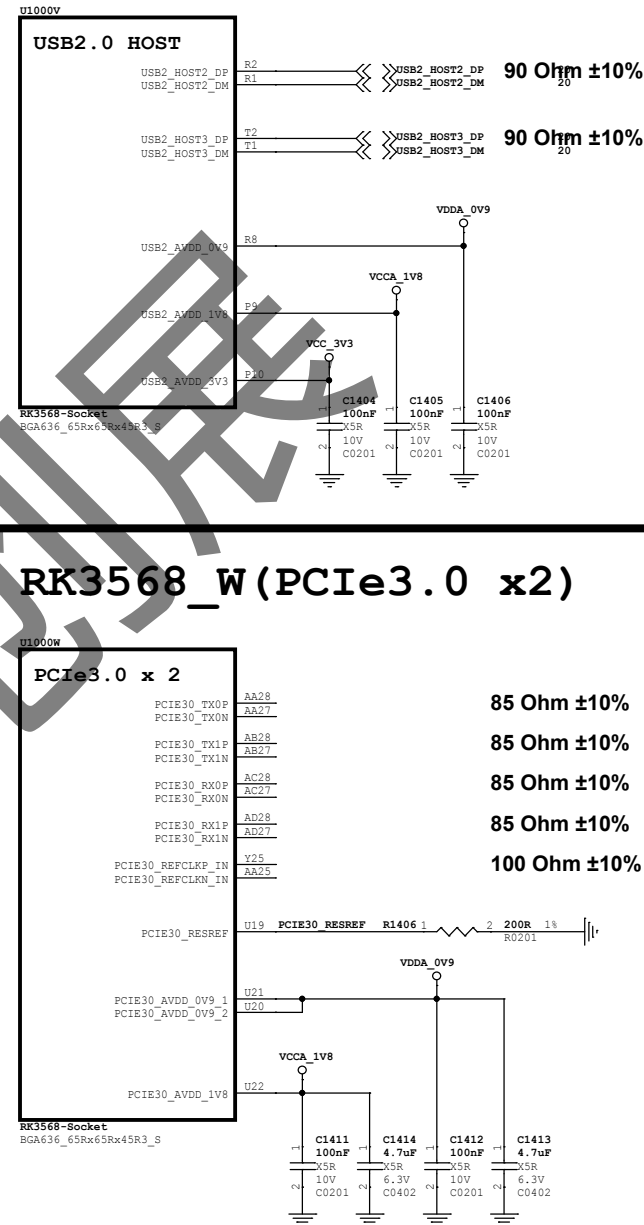
RK3568 V (USB2.0 HOST)



Note:

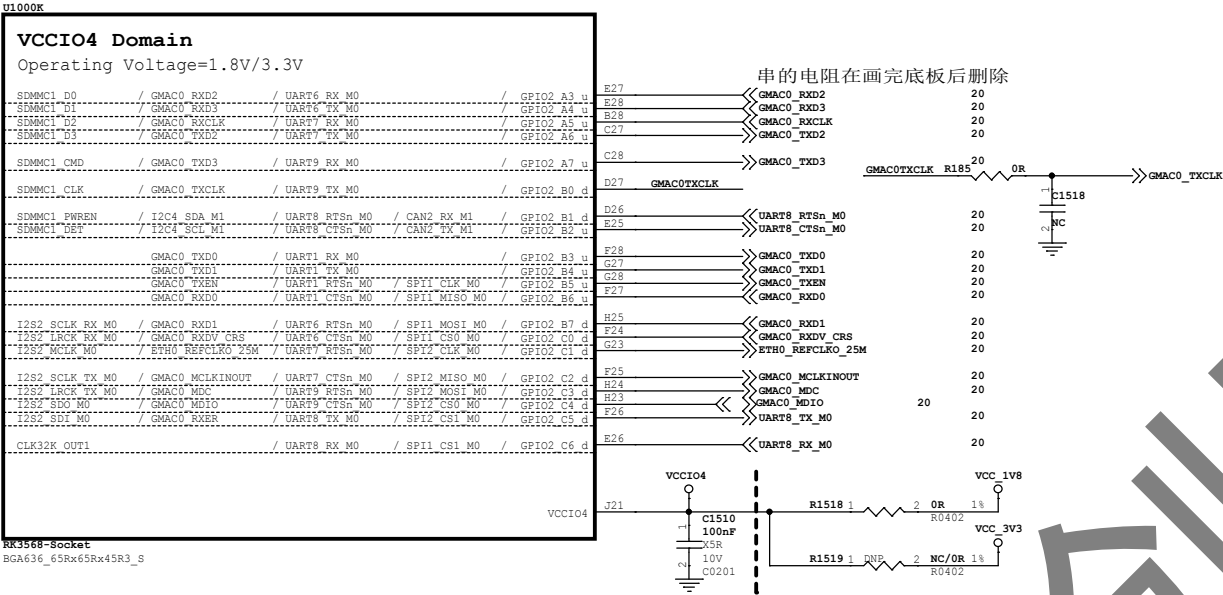
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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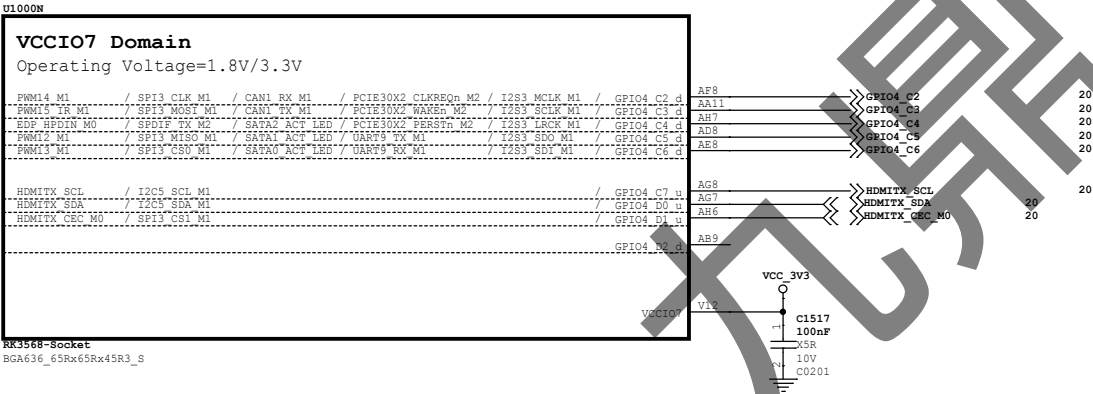


 瑞芯微电子		Rockchip Electronics Co., Ltd	
Project:	x3568cv1		
File:	07.RK3568_USB/PCIe/SATA PHY		
Date:	Monday, August 29, 2022		Rev.
Designed by:	Zhangzd	Reviewed by:	Default
		Sheet	7 of 17

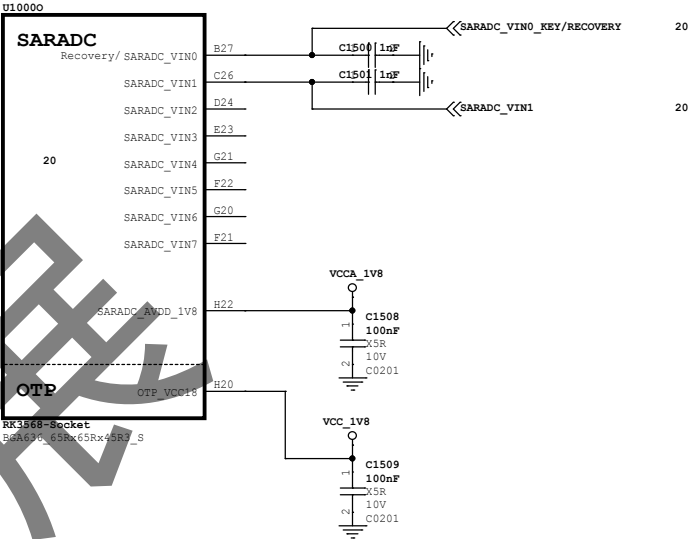
RK3568_K (VCCIO4 Domain)



RK3568_N (VCCIO7 Domain)



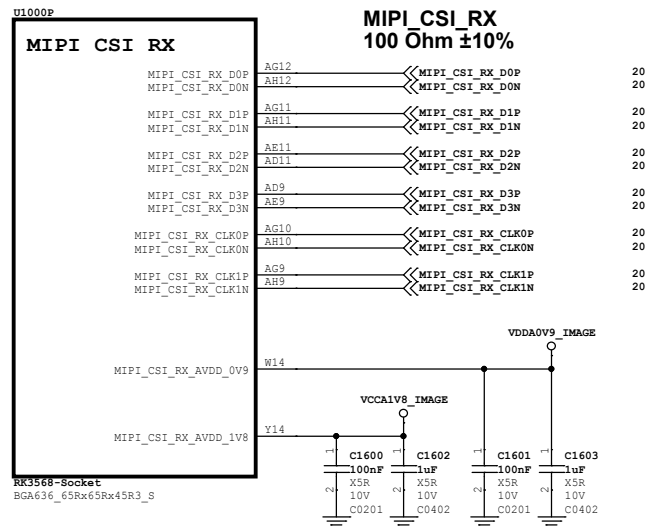
RK3568_O (SARADC/OTP)



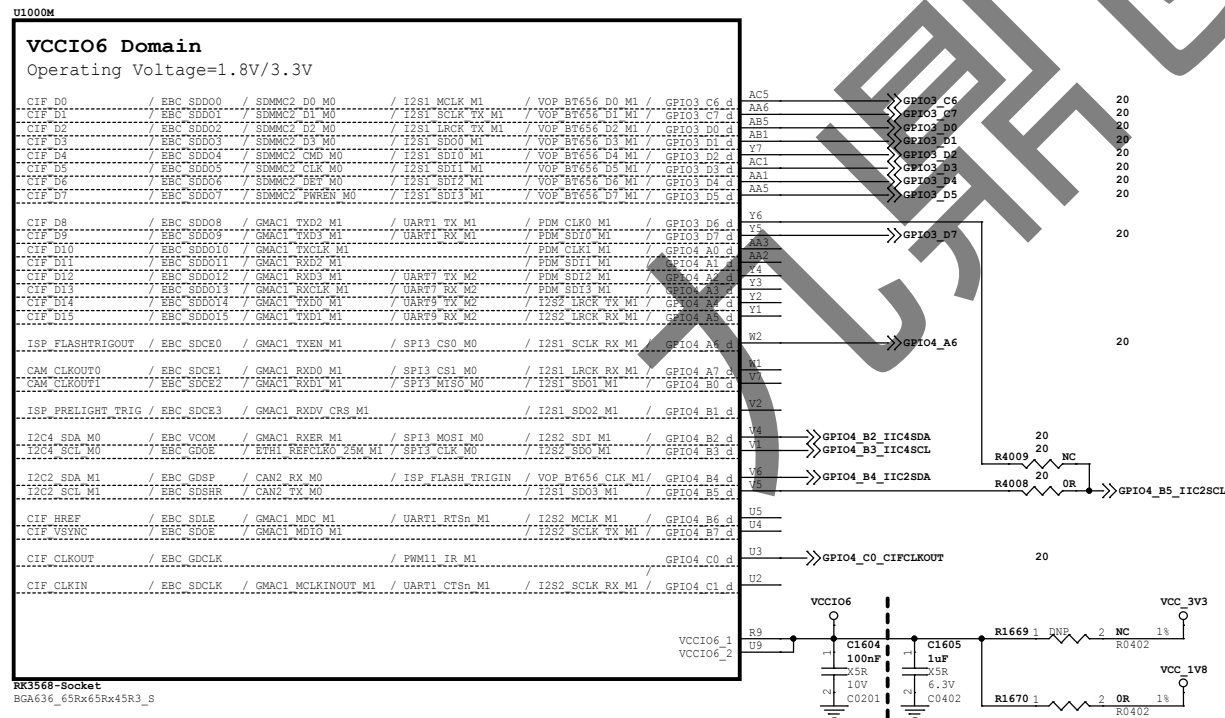
Note:
Caps of between dashed green lines
and U1000 should be placed under
the U1000 package

 瑞芯微电子		Rockchip Electronics Co., Ltd	
Project:		x3568cv1	
File:		08.RK3568_SARADC/GPIO	
Date:	Monday, August 29, 2022		Rev: V1.0
Designed by:	Zhangdz	Reviewed by:	Default
Sheet:	8		of 17

RK3568_P (MIPI_CSI_RX)



RK3568_M (VCCIO6 Domain)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

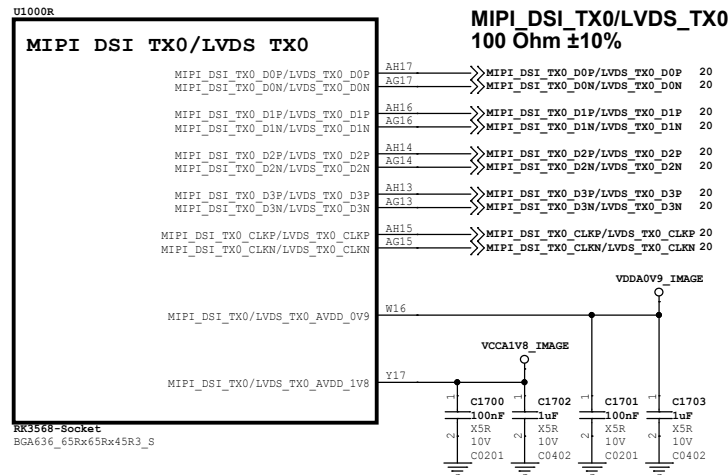
Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

Note:

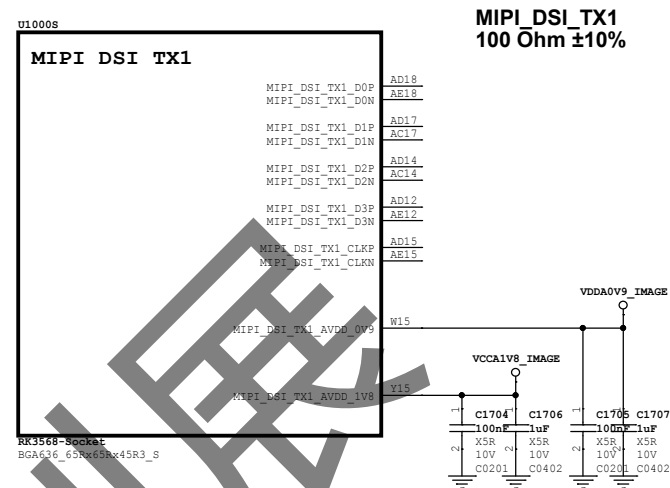
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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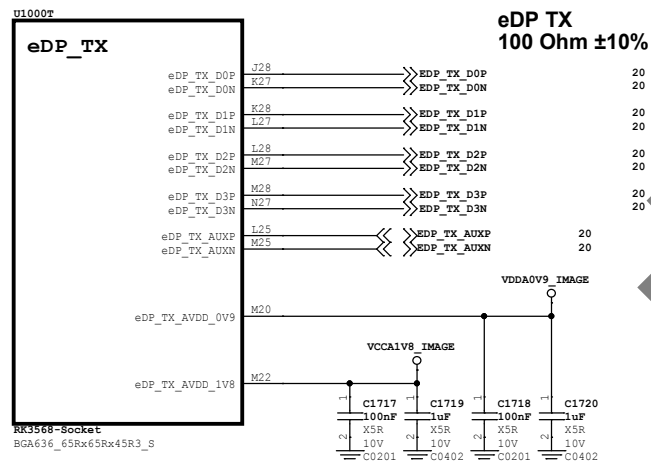
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)



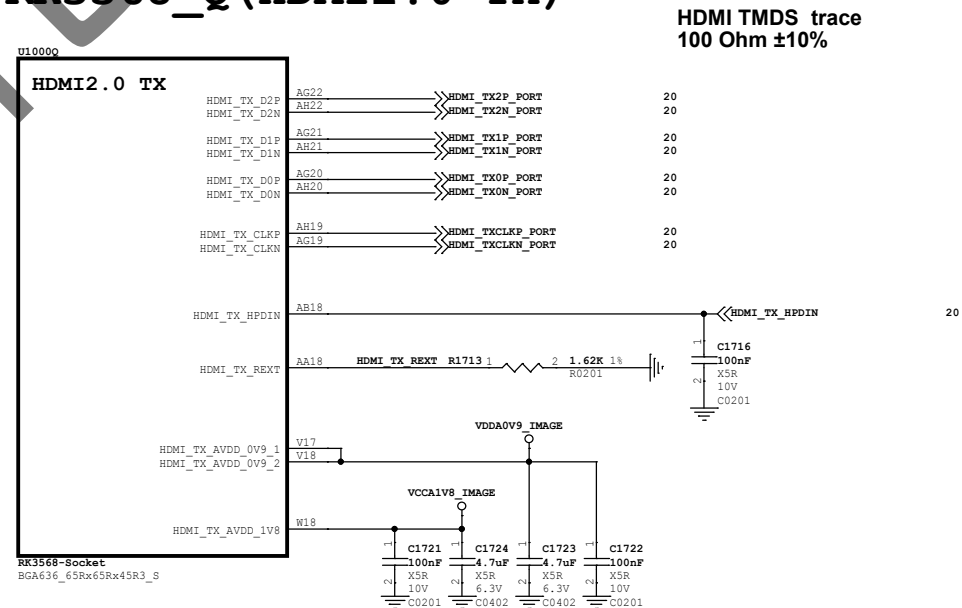
RK3568_T(eDP_TX)



Note:
 Caps of between dashed green lines and U1000 should be placed under the U1000 package.
 Other caps should be placed close to the U1000 package

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RK3568_Q(HDMI2.0 TX)



HDMI TMDs trace
 100 Ohm ±10%

 瑞芯微电子		Rockchip Electronics Co., Ltd	
Project:	x3568cv1		
File:	10.RK3568_VO Interface_1		
Date:	Monday, August 29, 2022		Rev: V1.0
Designed by:	Zhangtz	Reviewed by:	Default
Sheet:	10 of 17		

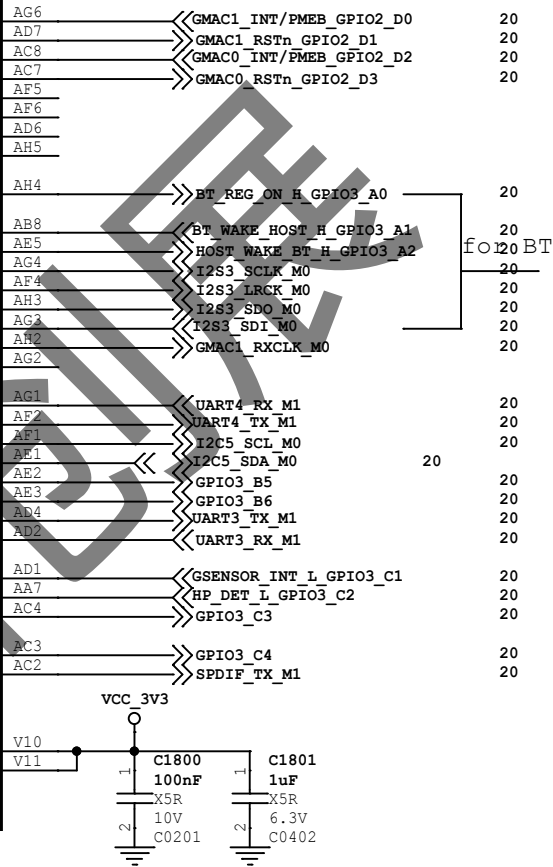
RK3568_L (VCCIO5 Domain)

U1000L

VCCIO5 Domain					
Operating Voltage=1.8V/3.3V					
LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREOn M1	/ I2S1 MCLK M2	/ GPIO2 D0 d
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEn M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 d
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE30X1 CLKREOn M1	/ I2S1 LRCK TX M2	/ GPIO2 D2 d
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE30X1 WAKEn M1	/ I2S1 SDI0 M2	/ GPIO2 D3 d
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREOn M1	/ I2S1 SDI1 M2	/ GPIO2 D4 d
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ I2S1 SDI2 M2	/ GPIO2 D5 d
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ I2S1 SDI3 M2	/ GPIO2 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ I2S1 SDO0 M2	/ GPIO2 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ I2S1 SDO1 M2	/ GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 d
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1	/ GPIO3 A5 d
LCDC D13	/ VOP BT1120 CLK	/ GMAC1 TXCLK M0	/ I2S3 SDI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d
LCDC D14	/ VOP BT1120 D5	/ GMAC1 RXCLK M0		/ SDMMC2 DET M1	/ GPIO3 A7 d
LCDC D15	/ VOP BT1120 D6	/ ETH1 REFCLK0 25M M0		/ SDMMC2 PWREN M1	/ GPIO3 B0 d
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ I2C5 SCL M0	/ PDM SDI0 M2	/ GPIO3 B3 d
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXER M0	/ I2C5 SDA M0	/ PDM SDI1 M2	/ GPIO3 B4 d
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C3 SCL M1	/ PWM10 M0	/ GPIO3 B5 d
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 d
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	/ GPIO3 B7 d
LCDC D23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	/ GPIO3 C0 d
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SDO2 M2	/ GPIO3 C1 d
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2	/ GPIO3 C2 d
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d
PWM15 IR M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LRCK RX M2	/ GPIO3 C5 d

VCCIO5_1
VCCIO5_2

RK3568-Socket
BGA636_65Rx65Rx45R3_S



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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 瑞芯微电子		Rockchip Electronics Co., Ltd			
Project:	x3568cv1				
File:	11.RK3568_VO Interface_2				
Date:	Monday, August 29, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	11 of 17

RK3568_H(VCCIO1 Domain)

U1000H

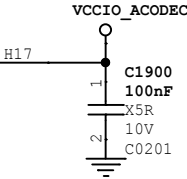
VCCIO1 Domain

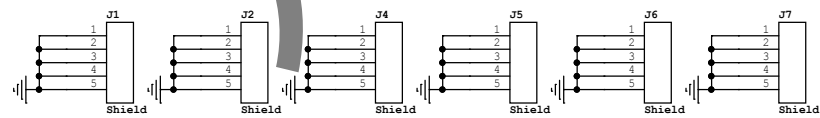
Operating Voltage=1.8V/3.3V

I2C3 SDA M0	/ UART3 RX M0	/ CAN1 RX M0	/ AUDIOPWM LOUT P	/ ACODEC ADC DATA	/ GPIO1 A0 u
I2C3 SCL M0	/ UART3 TX M0	/ CAN1 TX M0	/ AUDIOPWM LOUT N	/ ACODEC ADC CLK	/ GPIO1 A1 u
I2S1 MCLK M0	/ UART3 RTSn M0	/ SCR CLK	/ PCIE30X1 PERSTn M2		/ GPIO1 A2 d
I2S1 SCLK TX M0	/ UART3 CTSn M0	/ SCR IO	/ PCIE30X1 WAKEn M2	/ ACODEC DAC CLK	/ GPIO1 A3 d
I2S1 SCLK RX M0	/ UART4 RX M0	/ PDM CLK1 M0	/ SPDIF TX M0		/ GPIO1 A4 d
I2S1 LRCK TX M0	/ UART4 RTSn M0	/ SCR RST	/ PCIE30X1 CLKREQn M2	/ ACODEC DAC SYNC	/ GPIO1 A5 d
I2S1 LRCK RX M0	/ UART4 TX M0	/ PDM CLK0 M0	/ AUDIOPWM ROUT P		/ GPIO1 A6 d
I2S1 SDO0 M0	/ UART4 CTSn M0	/ SCR DET	/ AUDIOPWM ROUT N	/ ACODEC DAC DATAL	/ GPIO1 A7 d
I2S1 SDO1 M0	/ I2S1 SDI3 M0	/ PDM SDI3 M0	/ PCIE20 CLKREQn M2	/ ACODEC DAC DATAR	/ GPIO1 B0 d
I2S1 SDO2 M0	/ I2S1 SDI2 M0	/ PDM SDI2 M0	/ PCIE20 WAKEn M2	/ ACODEC ADC SYNC	/ GPIO1 B1 d
I2S1 SDO3 M0	/ I2S1 SDI1 M0	/ PDM SDI1 M0	/ PCIE20 PERSTn M2		/ GPIO1 B2 d
	I2S1 SDI0 M0	/ PDM SDI0 M0			/ GPIO1 B3 d

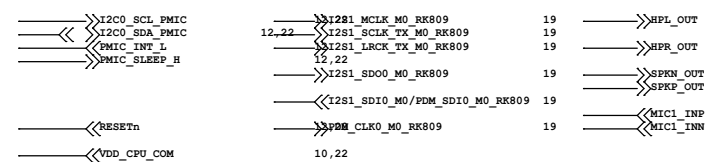
RK3568-Socket
BGA636_65Rx65Rx45R3_s

D18	<<	I2C3_SDA_M0	20
E18	>>	I2C3_SCL_M0	20
A19	>>	I2S1_MCLK_M0_RK809	21
B19	>>	I2S1_SCLK_TX_M0_RK809	21
F18			
A20	>>	I2S1_LRCK_TX_M0_RK809	21
C20	>>	PDM_CLK0_M0_RK809	21
B20	>>	I2S1_SDO0_M0_RK809	21
D20			
E20			
A21			
B21	<<	I2S1_SDIO_M0/PDM_SDIO_M0_RK809	21

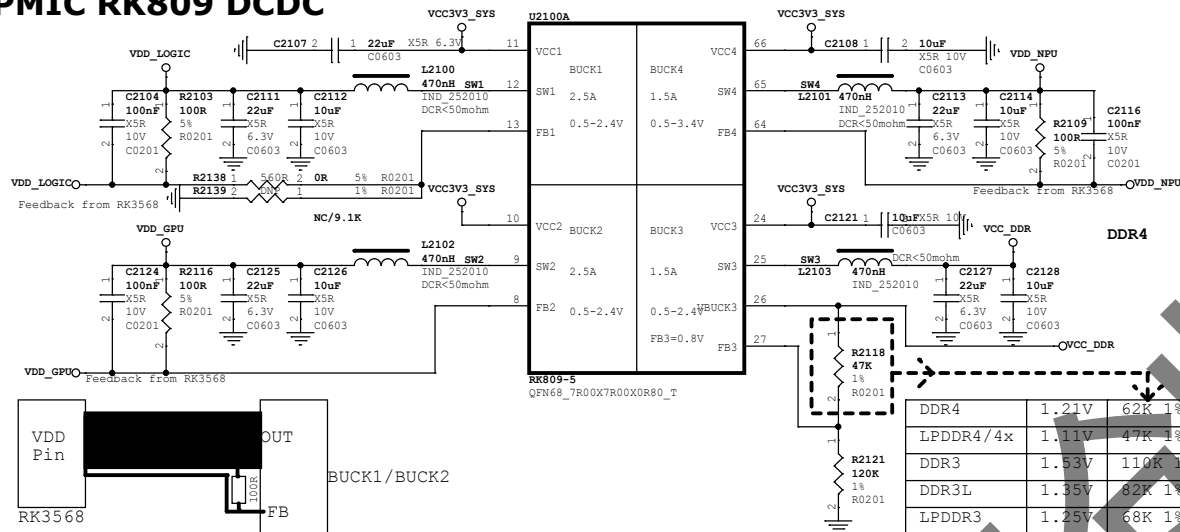




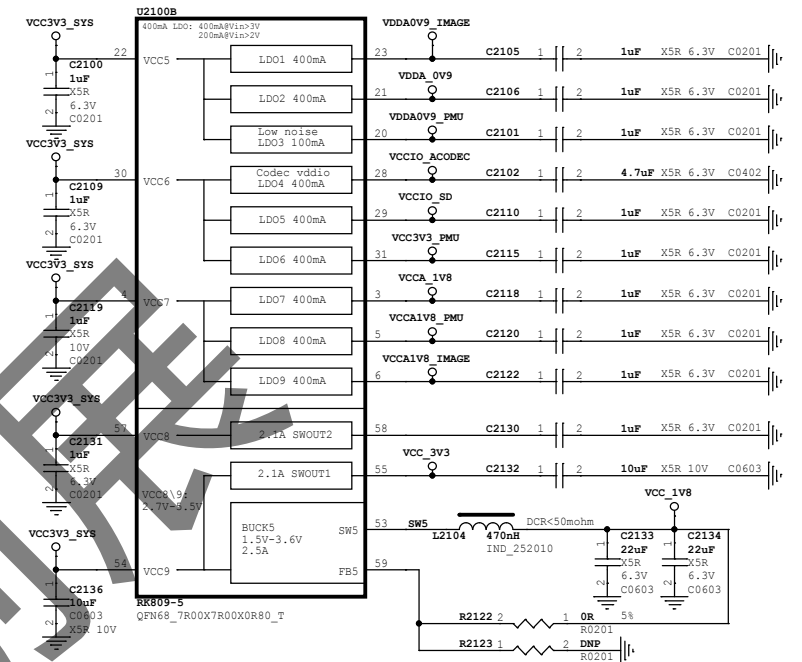
 瑞芯微电子		Rockchip Electronics Co., Ltd		
Project:	x3568cv1			
File:	16.Connector			
Date:	Monday, August 29, 2022		Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet: 16 of 17



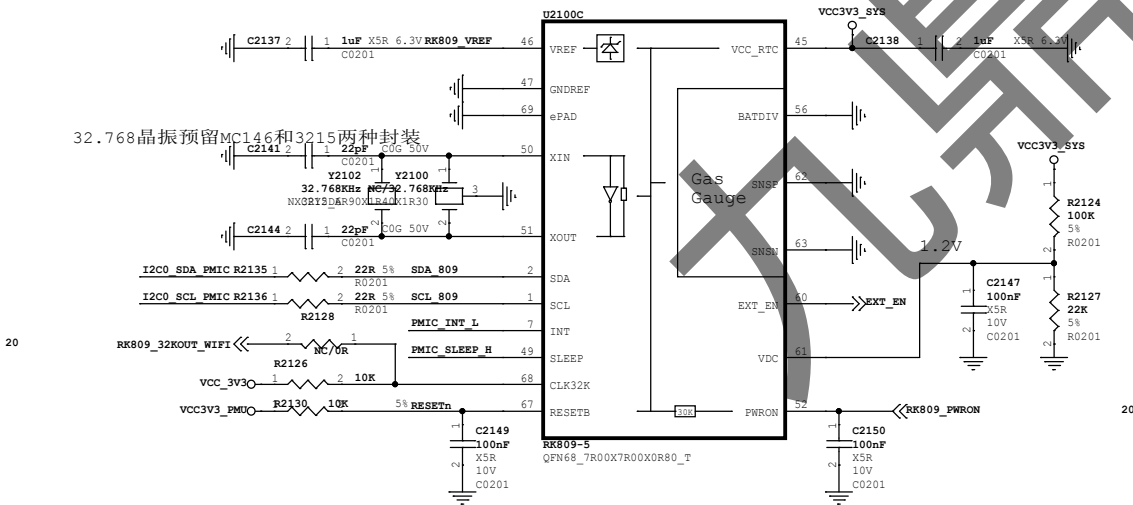
PMIC RK809 DCDC



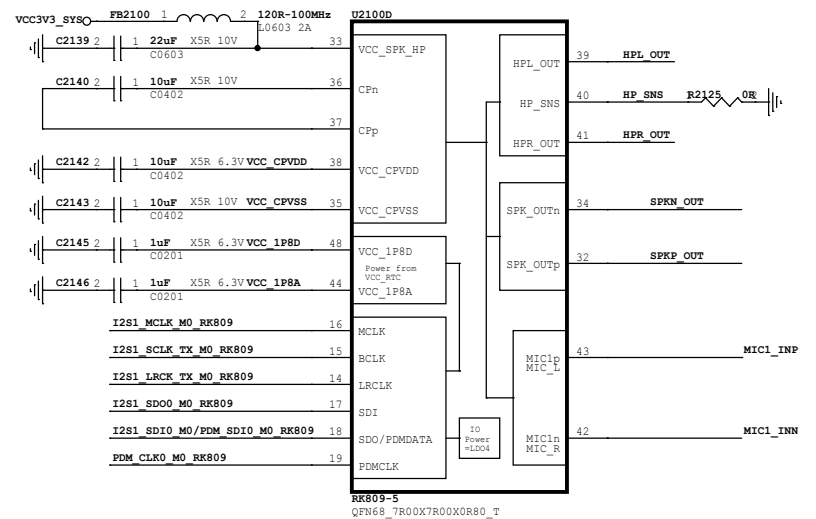
PMIC RK809 LDO



PMIC RK809 Managerment

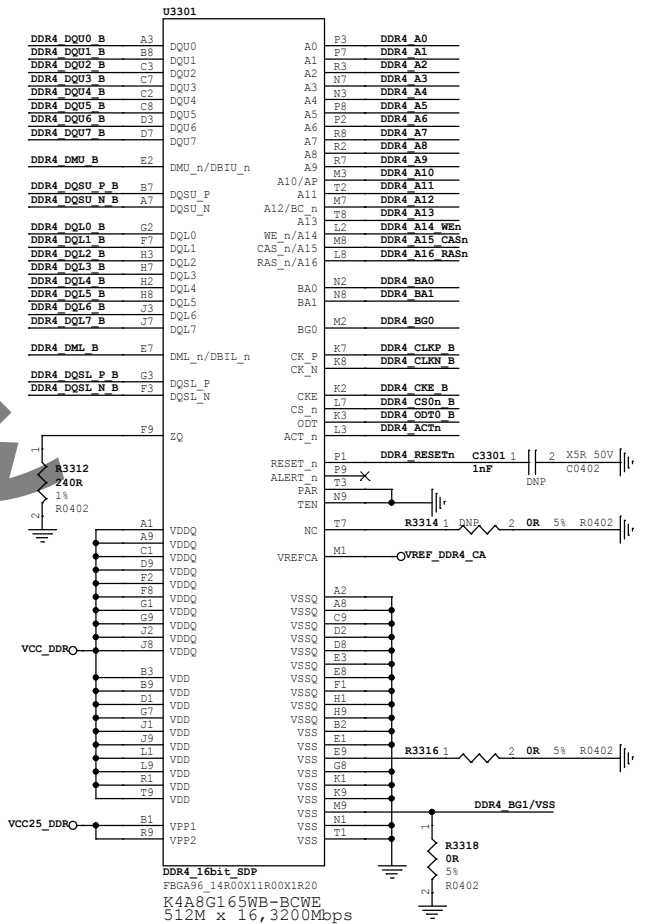
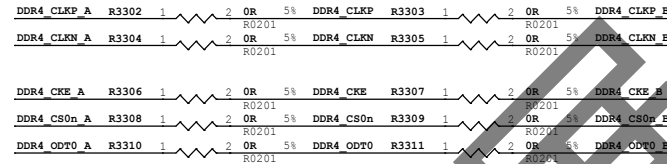
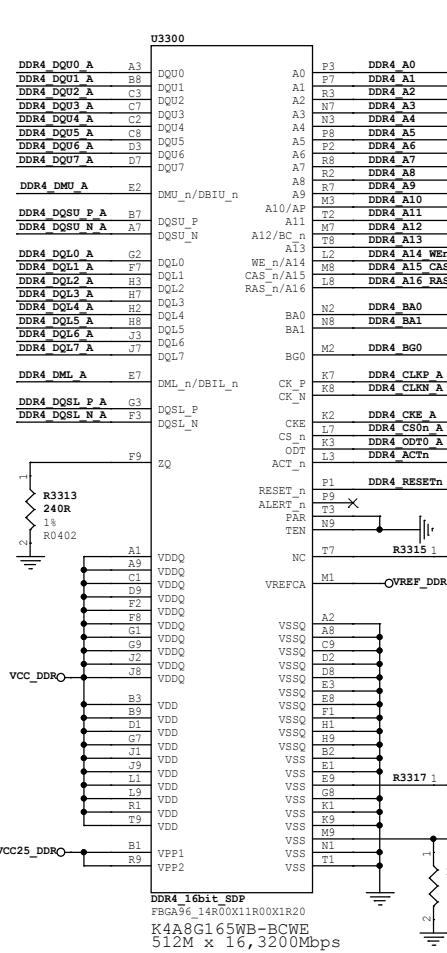


PMIC RK809 CODEC

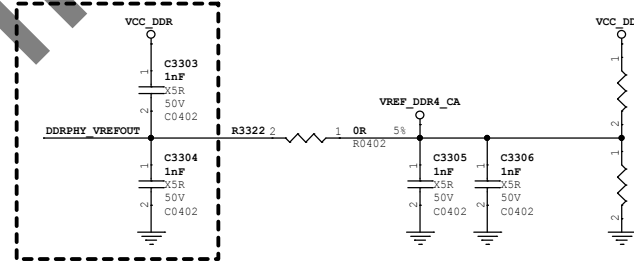


The schematic diagram illustrates the DCDC power supply circuit for the RK3568. The main components include the U2200 DCDC converter, the TCS4525 PMIC, and various passive components like resistors, capacitors, and an inductor. The input is 12V, and the output is VDD for the RK3568. A feedback loop is shown with a 100R resistor and a connection to the RK3568's VDD pin.

DDR4P216SD6



Notes:
Close to SOC



Notes:
Close to DRAM

Notes:
When use DDP DDR4 SDRAM,
DDR4 SDRAM' M9 pin connect to DDR_BG1 net of SOC;
DDR4 SDRAM' T7 pin connect to GND;
DDR4 SDRAM' E9 pin connect to GND by 240ohm resistor

