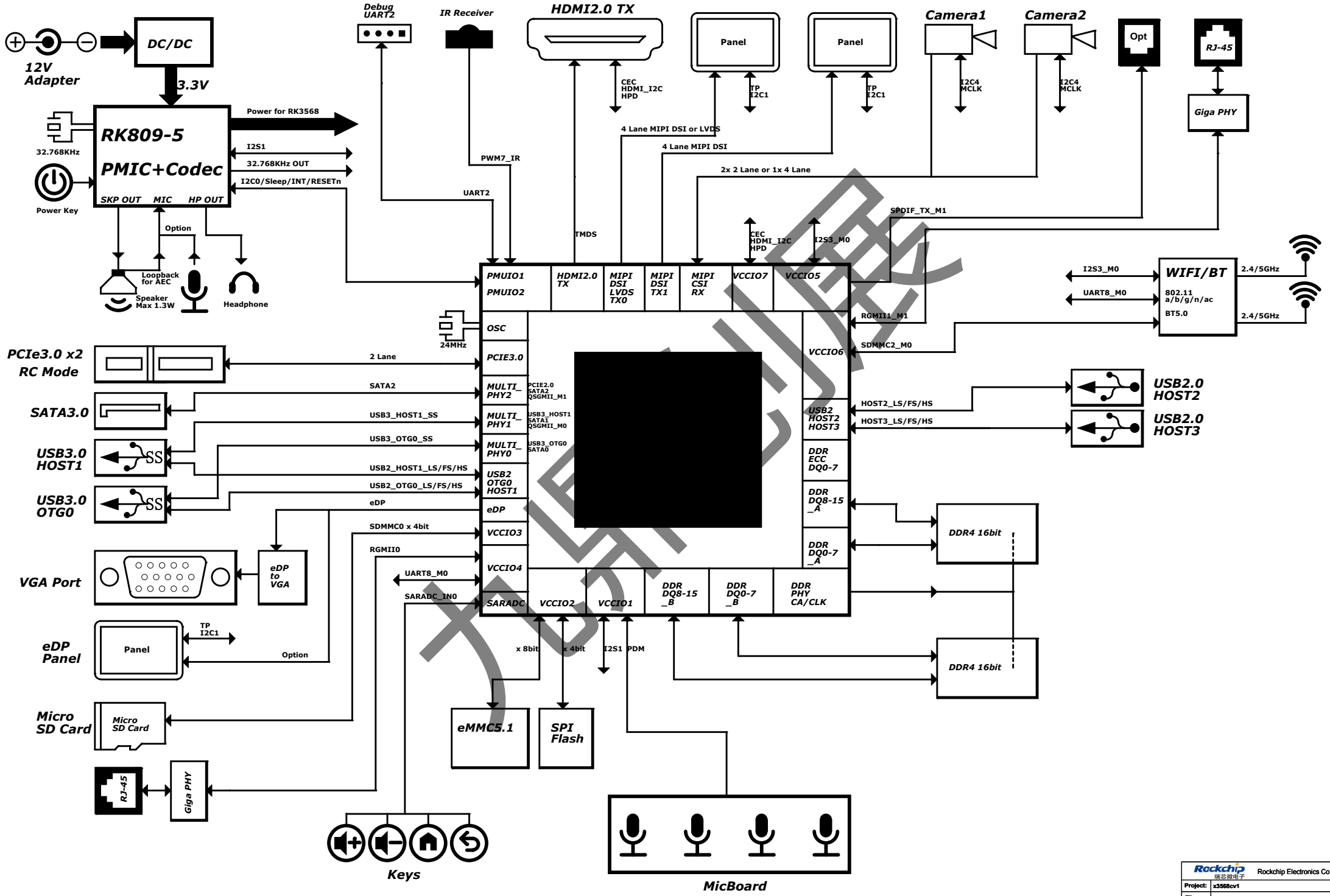
RK3568 Ref Block Diagram



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	x3568cv1
File:	01.title
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Reviewed by:	Default
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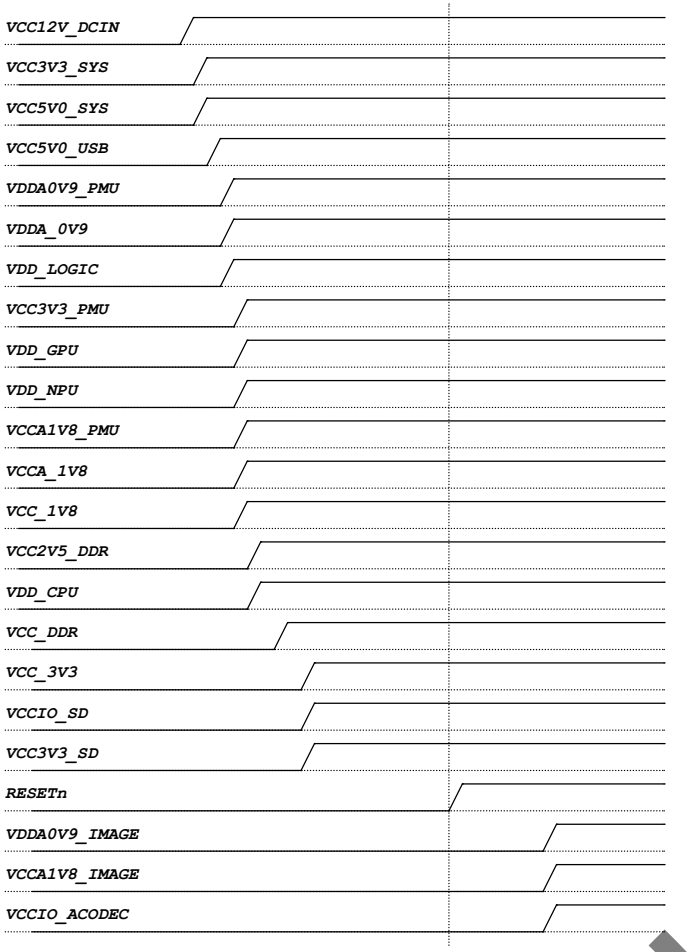
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	OFF	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	ON	TBD	TBD

IO Power Domain Map
Updates must be Revision accordingly!

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

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Project:	x3568cv1				
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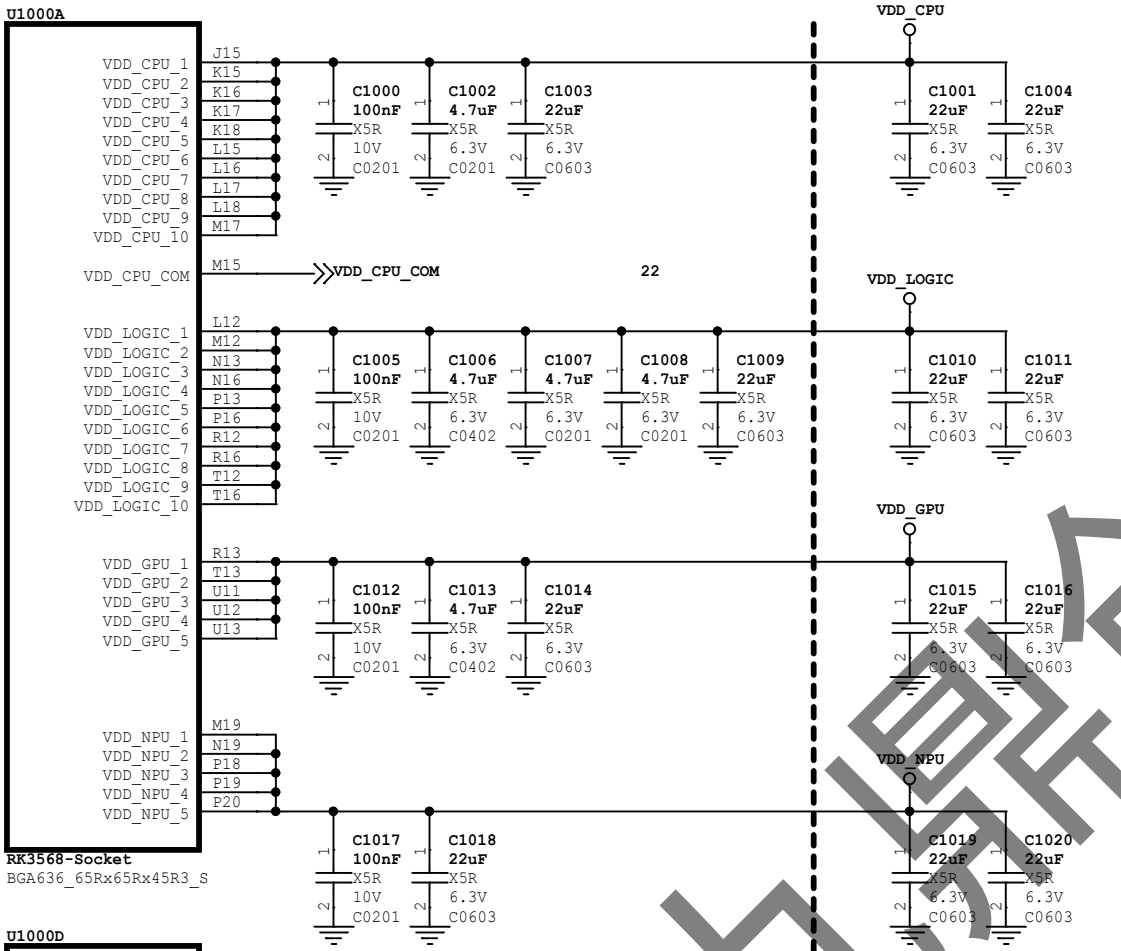
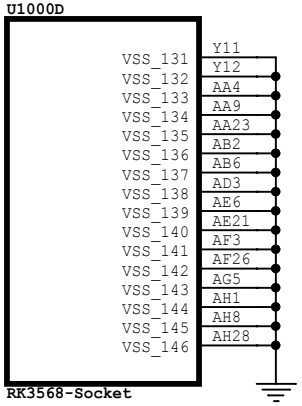
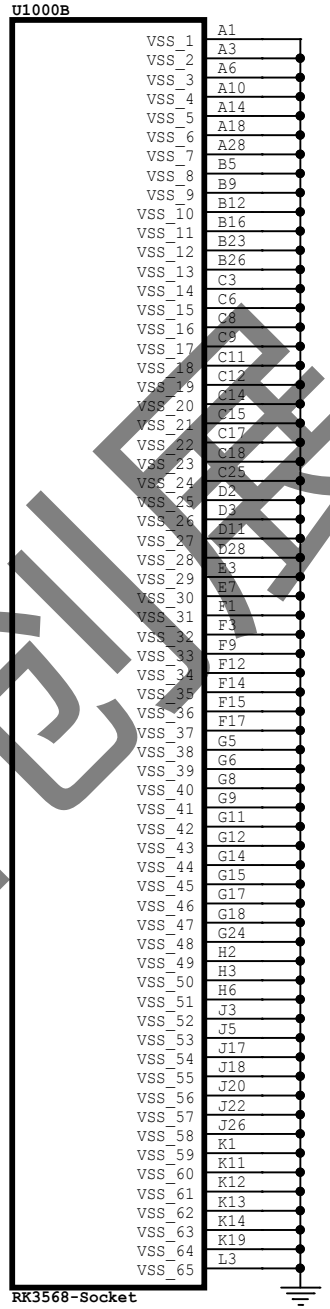
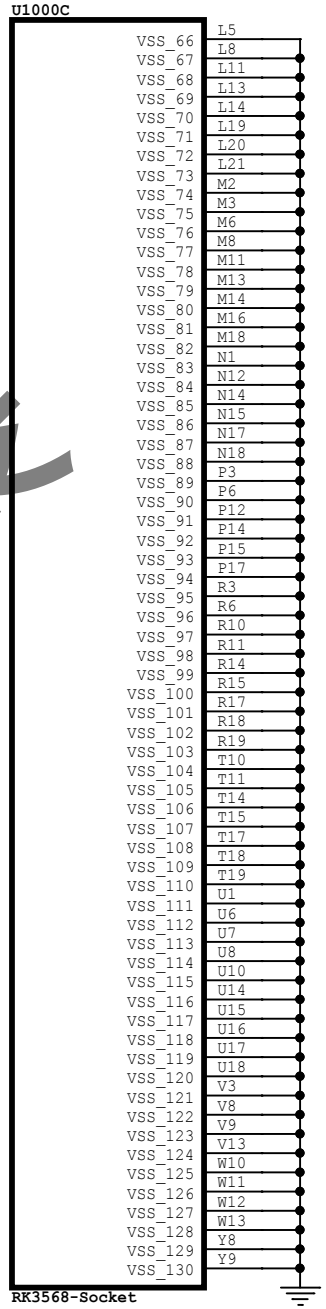
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	2 of 17

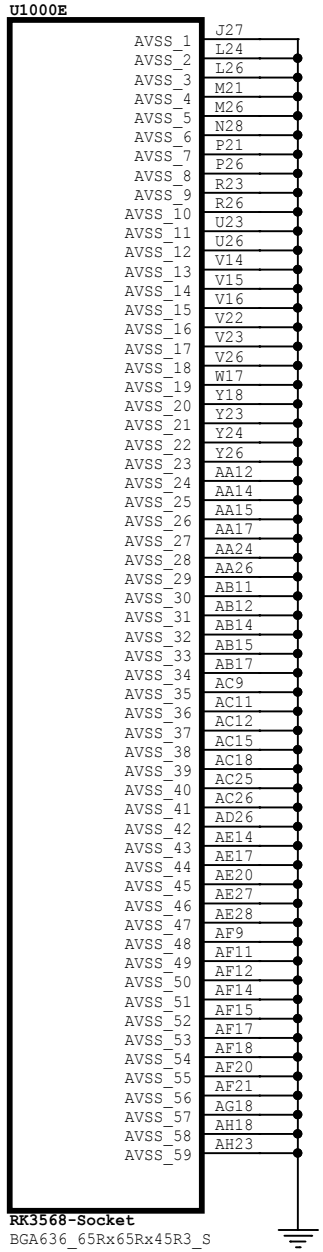
RK3568_ABCDE (Power&Gnd)











Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	03.RK3568_Power/GND				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	3 of 17

RK3568_F (DDR PHY)

U1000F

DDR4	LPDDR4	DDR3	LPDDR3	BGA636
DDR_DQ0_A	DDR4_DQL0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ15	F2
DDR_DQ1_A	DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ14	E1
DDR_DQ2_A	DDR4_DQL4_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ10	E2
DDR_DQ3_A	DDR4_DQL6_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ9	D1
DDR_DQ4_A	DDR4_DQL7_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ13	J1
DDR_DQ5_A	DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ12	J2
DDR_DQ6_A	DDR4_DQL3_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ8	H1
DDR_DQ7_A	DDR4_DQL1_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ11	H4
DDR_DM0_A	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1	H5
DDR_DQS0P_A	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS1P	G1
DDR_DQS0N_A	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS1N	G2
DDR_DQ8_A	DDR4_DQU3_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ25	M1
DDR_DQ9_A	DDR4_DQU1_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ24	N2
DDR_DQ10_A	DDR4_DQU7_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ28	L7
DDR_DQ11_A	DDR4_DQU5_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ29	L6
DDR_DQ12_A	DDR4_DQU2_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ26	K2
DDR_DQ13_A	DDR4_DQU4_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ31	J6
DDR_DQ14_A	DDR4_DQU6_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ30	J7
DDR_DQ15_A	DDR4_DQU0_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ27	L4
DDR_DM1_A	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM3	J4
DDR_DQS1P_A	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS3P	L2
DDR_DQS1N_A	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS3N	L1
DDR_DQ0_B	DDR4_DQU7_B	LPDDR4_DQ0_B	DDR3_DQ16	LPDDR3_DQ1	B10
DDR_DQ1_B	DDR4_DQU5_B	LPDDR4_DQ1_B	DDR3_DQ17	LPDDR3_DQ5	A9
DDR_DQ2_B	DDR4_DQU3_B	LPDDR4_DQ2_B	DDR3_DQ18	LPDDR3_DQ6	D12
DDR_DQ3_B	DDR4_DQU1_B	LPDDR4_DQ3_B	DDR3_DQ19	LPDDR3_DQ4	E12
DDR_DQ4_B	DDR4_DQU0_B	LPDDR4_DQ4_B	DDR3_DQ20	LPDDR3_DQ2	A12
DDR_DQ5_B	DDR4_DQU6_B	LPDDR4_DQ5_B	DDR3_DQ21	LPDDR3_DQ3	D15
DDR_DQ6_B	DDR4_DQU4_B	LPDDR4_DQ6_B	DDR3_DQ22	LPDDR3_DQ7	E15
DDR_DQ7_B	DDR4_DQU2_B	LPDDR4_DQ7_B	DDR3_DQ23	LPDDR3_DQ0	E14
DDR_DM0_B	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM2	LPDDR3_DM0	D14
DDR_DQS0P_B	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS2P	LPDDR3_DQS0P	A11
DDR_DQS0N_B	DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS2N	LPDDR3_DQS0N	B11
DDR_DQ8_B	DDR4_DQL0_B	LPDDR4_DQ8_B	DDR3_DQ24	LPDDR3_DQ18	A16
DDR_DQ9_B	DDR4_DQL2_B	LPDDR4_DQ9_B	DDR3_DQ25	LPDDR3_DQ19	B17
DDR_DQ10_B	DDR4_DQL4_B	LPDDR4_DQ10_B	DDR3_DQ26	LPDDR3_DQ22	A17
DDR_DQ11_B	DDR4_DQL6_B	LPDDR4_DQ11_B	DDR3_DQ27	LPDDR3_DQ20	B18
DDR_DQ12_B	DDR4_DQL7_B	LPDDR4_DQ12_B	DDR3_DQ28	LPDDR3_DQ21	B13
DDR_DQ13_B	DDR4_DQL5_B	LPDDR4_DQ13_B	DDR3_DQ29	LPDDR3_DQ17	A13
DDR_DQ14_B	DDR4_DQL1_B	LPDDR4_DQ14_B	DDR3_DQ30	LPDDR3_DQ23	D17
DDR_DQ15_B	DDR4_DQL3_B	LPDDR4_DQ15_B	DDR3_DQ31	LPDDR3_DQ16	B14
DDR_DM1_B	DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM3	LPDDR3_DM2	E17
DDR_DQS1P_B	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS3P	LPDDR3_DQS2P	B15
DDR_DQS1N_B	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS3N	LPDDR3_DQS2N	A15
DDR_ECC_DQ0	DDR4_ECC_DQ7	--	DDR3_ECC_DQ0		P5
DDR_ECC_DQ1	DDR4_ECC_DQ0	--	DDR3_ECC_DQ1		M4
DDR_ECC_DQ2	DDR4_ECC_DQ2	--	DDR3_ECC_DQ2		M5
DDR_ECC_DQ3	DDR4_ECC_DQ1	--	DDR3_ECC_DQ3		R5
DDR_ECC_DQ4	DDR4_ECC_DQ6	--	DDR3_ECC_DQ4		M7
DDR_ECC_DQ5	DDR4_ECC_DQ4	--	DDR3_ECC_DQ5		R7
DDR_ECC_DQ6	DDR4_ECC_DQ3	--	DDR3_ECC_DQ6		P4
DDR_ECC_DQ7	DDR4_ECC_DQ5	--	DDR3_ECC_DQ7		R4
DDR_ECC_DM	DDR4_ECC_DM	--	DDR3_ECC_DM		P7
DDR_ECC_DQS_P	DDR4_ECC_DQS_P	--	DDR3_ECC_DQS_P		P2
DDR_ECC_DQS_N	DDR4_ECC_DQS_N	--	DDR3_ECC_DQS_N		P1

RK3568-Socket
BGA636_65Rx65Rx45R3_S

DDR4	LPDDR4	DDR3	LPDDR3	BGA636
DDR4_A0	LPDDR4_CLKP_B	DDR3_A9	---	AC0	B6
DDR4_A1	---	DDR3_A2	---	AC1	F5
DDR4_A2	LPDDR4_A1_A	DDR3_A4	LPDDR3_A6	AC2	B1
DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	---	AC3	F4
DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3	AC4	D9
DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2	AC5	B7
DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1	AC6	A7
DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	---	AC7	A8
DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9	AC8	C1
DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	---	AC9	A5
DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---	AC10	D6
DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A8	AC11	C2
DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---	AC12	C4
DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0	AC13	B8
DDR4_A14_WEn	LPDDR4_A4_A	DDR3_A12	LPDDR3_A5	AC14	C5
DDR4_A15_CASn	LPDDR4_A2_A	DDR3_A15	---	AC15	E4
DDR4_A16_RASn	LPDDR4_A5_A	DDR3_RASn	LPDDR3_A7	AC16	D5
DDR4_ACTn	LPDDR4_CKE1_B	DDR3_CASn	---	AC17	E6
DDR4_BA0	LPDDR4_A2_B	DDR3_A1	---	AC18	E11
DDR4_BA1	LPDDR4_A4_B	DDR3_A0	LPDDR3_A4	AC19	E9
DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_WEn	---	AC20	E8
DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	---	AC21	F7
DDR4_CKE	LPDDR4_CKE0_A	DDR3_BA2	LPDDR3_CKE	AC22	B3
DDR4_CLKP	LPDDR4_CLKP_A	DDR3_CLKP	LPDDR3_CLKP	AC23	B4
DDR4_CLKN	LPDDR4_CLKN_A	DDR3_CLKN	LPDDR3_CLKN	AC24	A4
DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0	AC25	A2
DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CS1n	LPDDR3_ODT1	AC26	B2
DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	LPDDR3_CS1n	AC27	E8
DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	LPDDR3_CS0n	AC28	D8
DDR4_RESETn	LPDDR4_RESETn	DDR3_RESETn	---	AC29	F11

Note: Sequences can not be swap

Note:
Except DDR3, other DQ sequences can not be swap

DDR3L	=1.35V
DDR3	=1.5V
DDR4	=1.2V
LPDDR3	=1.2V
LPDDR4	=1.1V
LPDDR4x	=1.1V

DDRPHY_VDDQ_1
DDRPHY_VDDQ_2
DDRPHY_VDDQ_3
DDRPHY_VDDQ_4
DDRPHY_VDDQ_5
DDRPHY_VDDQ_6
DDRPHY_VDDQ_7
DDRPHY_VDDQ_8

DDR3L	=1.35V
DDR3	=1.5V
DDR4	=1.2V
LPDDR3	=1.2V
LPDDR4	=1.1V
LPDDR4x	**=0.6V**

DDRPHY_VDDQL_1
DDRPHY_VDDQL_2
DDRPHY_VDDQL_3
DDRPHY_VDDQL_4
DDRPHY_VDDQL_5
DDRPHY_VDDQL_6

DDR_RZQ
DDR_VREFOUT
DDR_AVSS

DDR_RZQ — R1100 1% 120R 0201 — VCC_DDR

For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin

LPDDR4/LPDDR4x 1.1V

VCC_DDR

C1100 100nF X5R 10V C0201	C1101 100nF X5R 10V C0201	C1102 4.7uF X5R 6.3V C0402	C1103 100nF X5R 10V C0402	C1104 10uF X5R 10V C0603

VCC0V6_DDR

C1105 100nF X5R 10V C0201	C1106 100nF X5R 10V C0201	C1107 4.7uF X5R 6.3V C0402	C1108 4.7uF X5R 6.3V C0402	C1109 4.7uF X5R 6.3V C0402

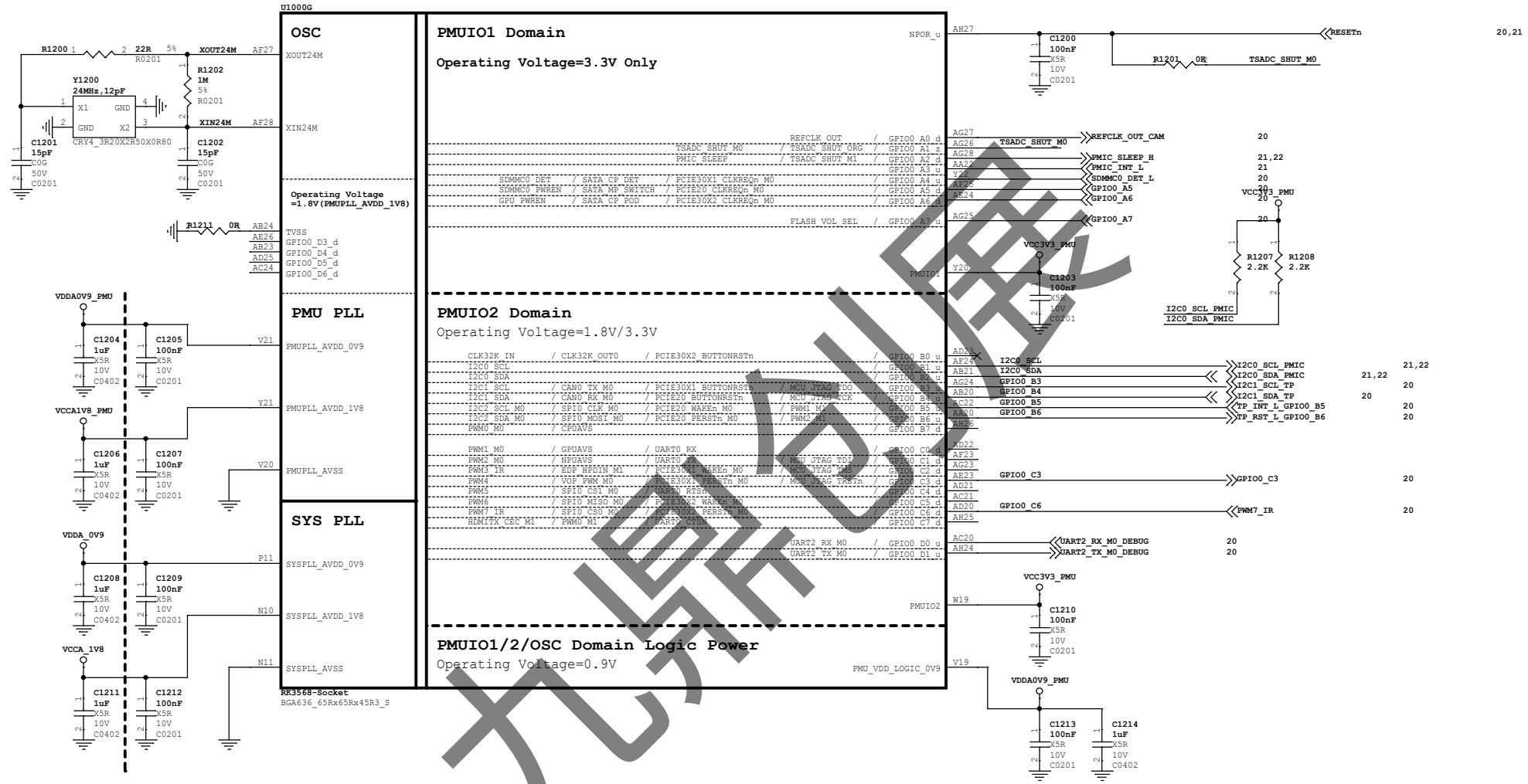
LPDDR4X

Note:

Caps should be placed under the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	x3568cv1		
File:	04.RK3568_DDR PHY		
Date:	Thursday, June 16, 2022	Rev:	V1.0
Designed by:	Zhangdz	Reviewed by: Default	Sheet: 4 of 17

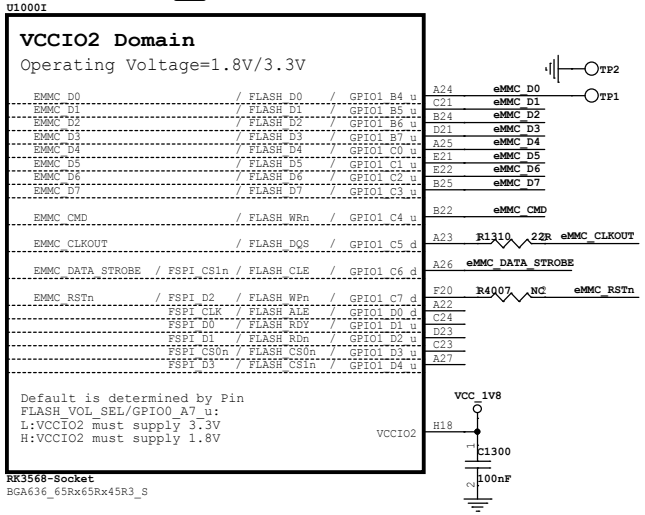
RK3568_G(OSC/PLL/PMUIO1/2)



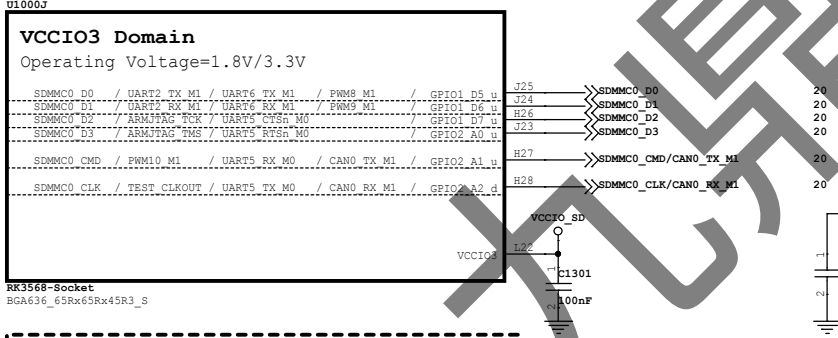
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	05.RK3568_OSC/PLL/PMUIO				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	5 of 17

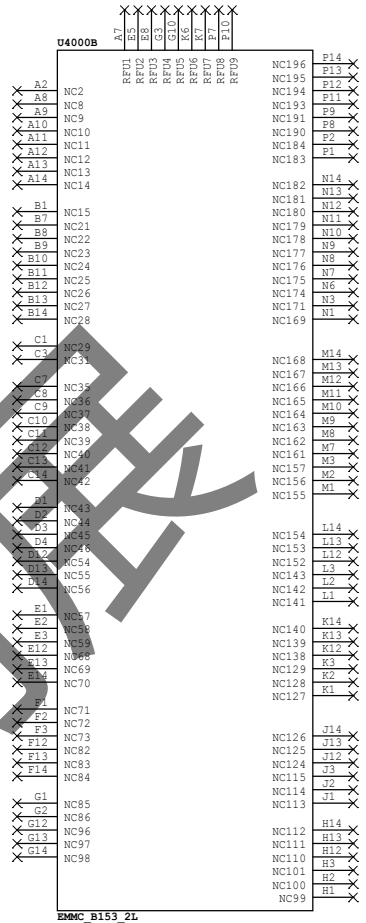
RK3568_I(VCCIO2 Domain)

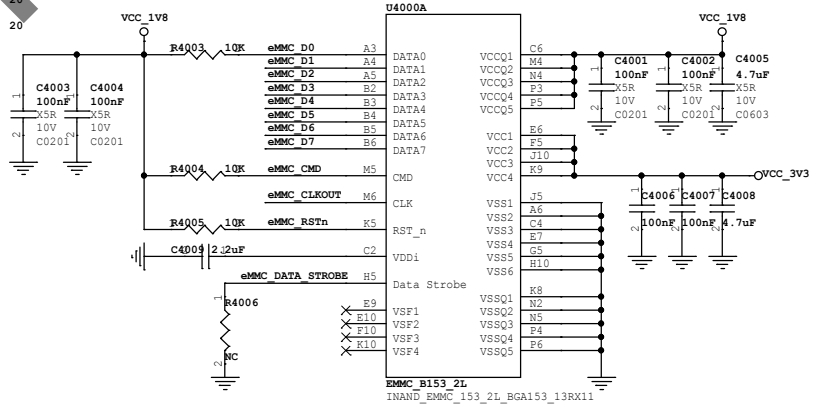


RK3568_J(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

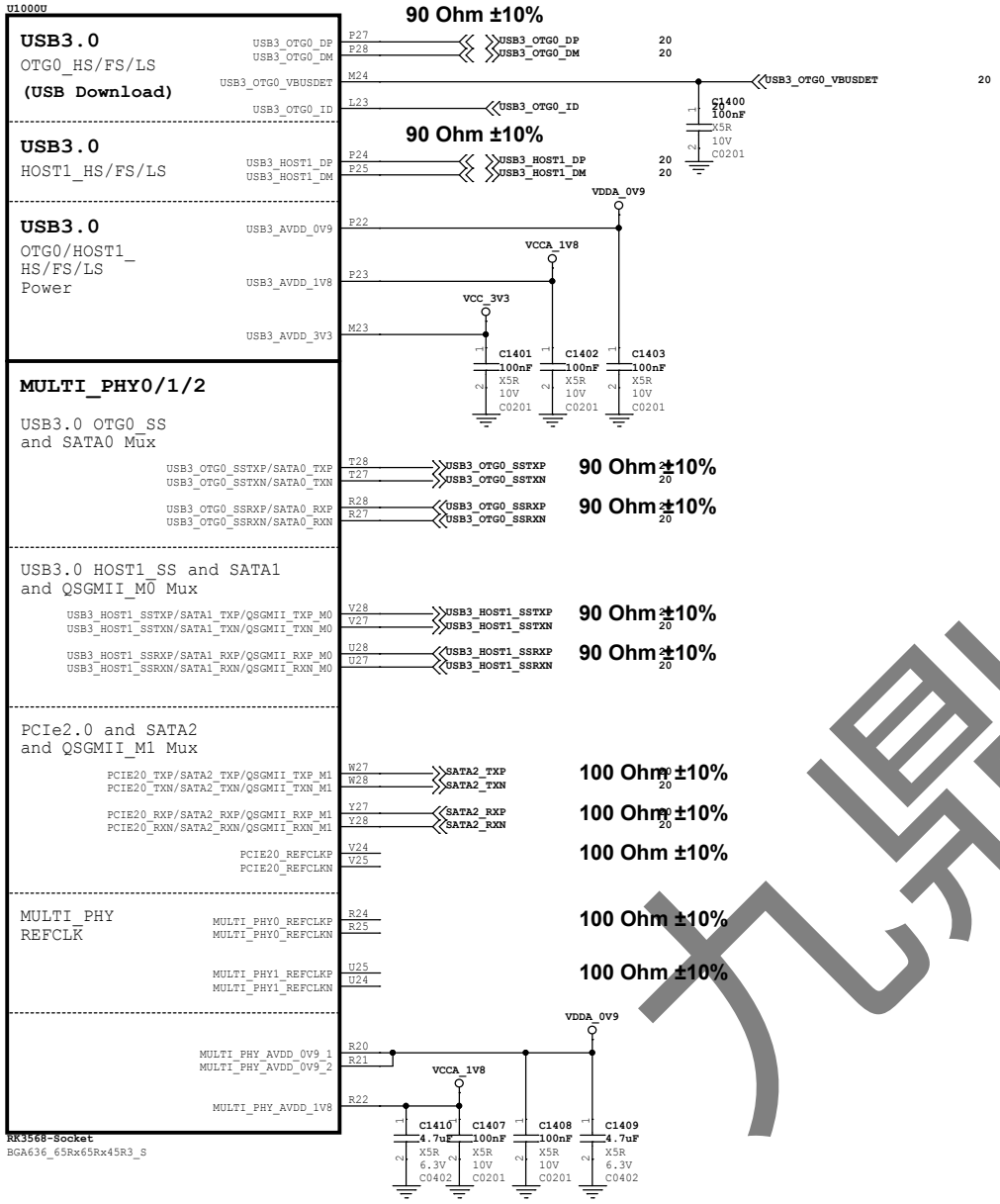




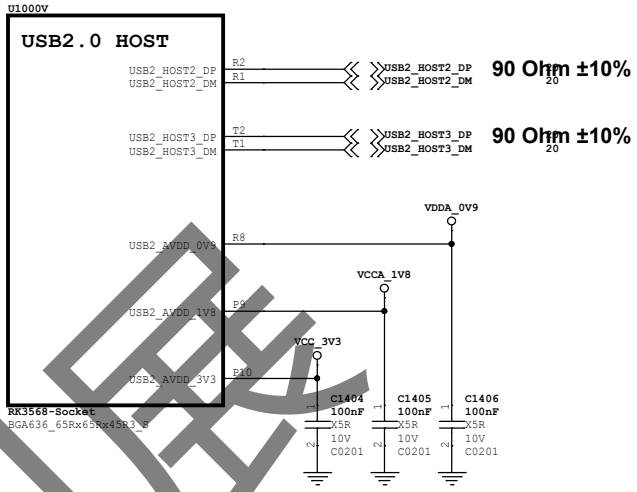
EMMC管脚定义，和3288原理图中EMMC定义不同，注意封装

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	06.RK3568_Flash/SD Controller				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	6 of 17

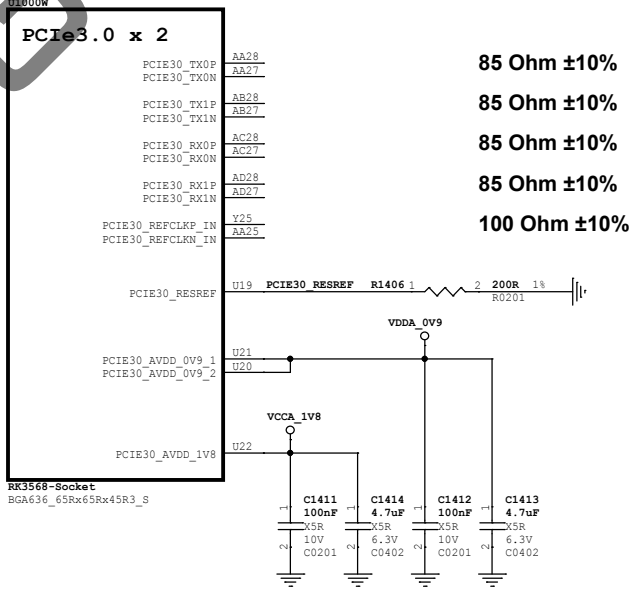
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)

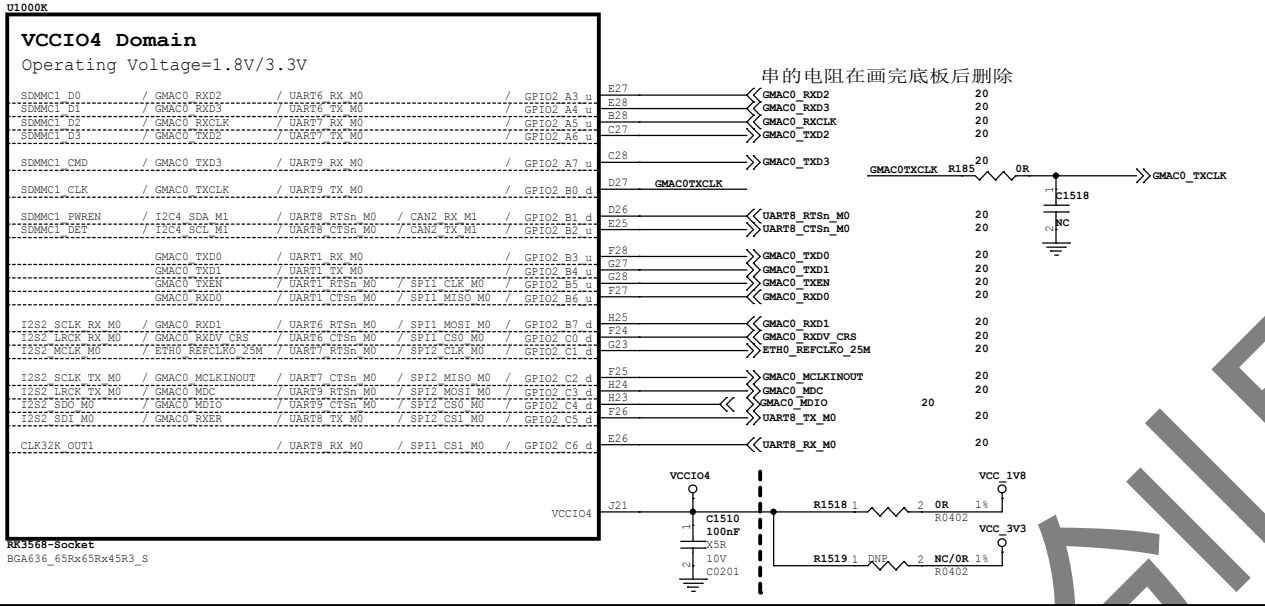


Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

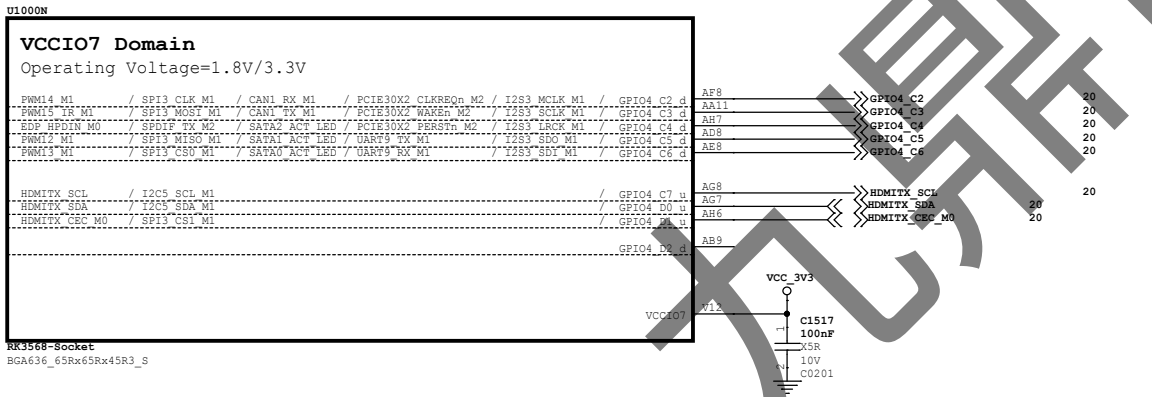
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	07.RK3568_USB/PCIe/SATA PHY				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	7 of 17

RK3568_K(VCCIO4 Domain)

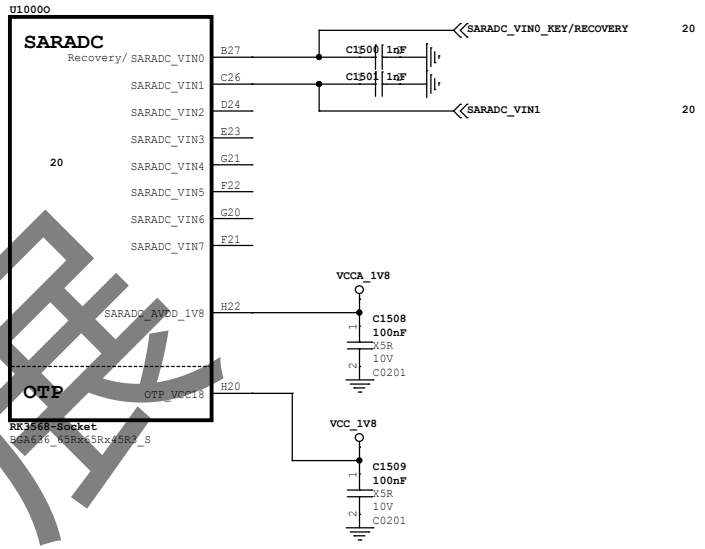


串的电阻在画完底板后删除

RK3568_N(VCCIO7 Domain)



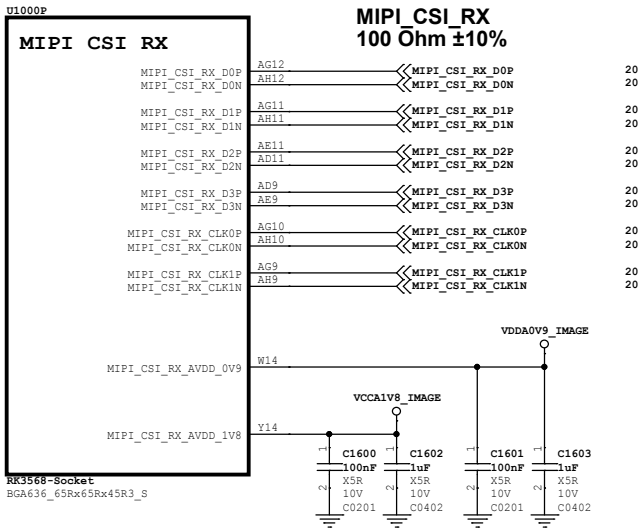
RK3568_O(SARADC/OTP)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	08.RK3568_SARADC/GPIO				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	8 of 17

RK3568_P(MIPI_CSI_RX)

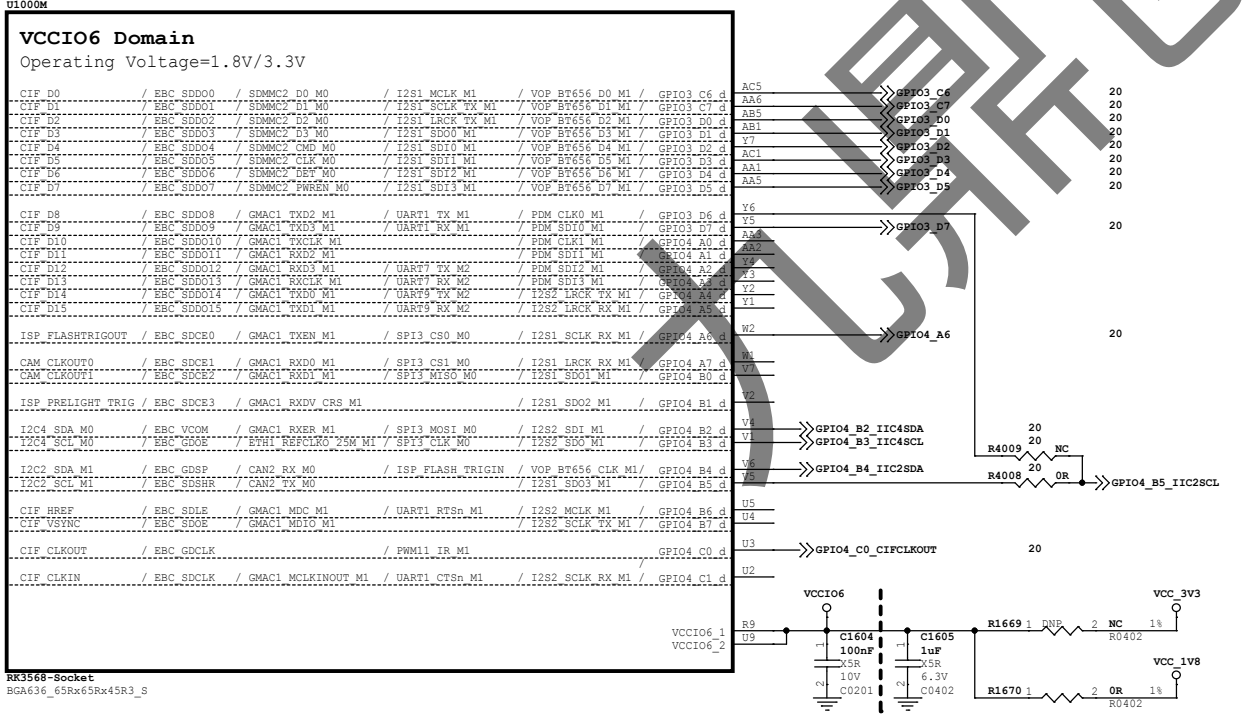


Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

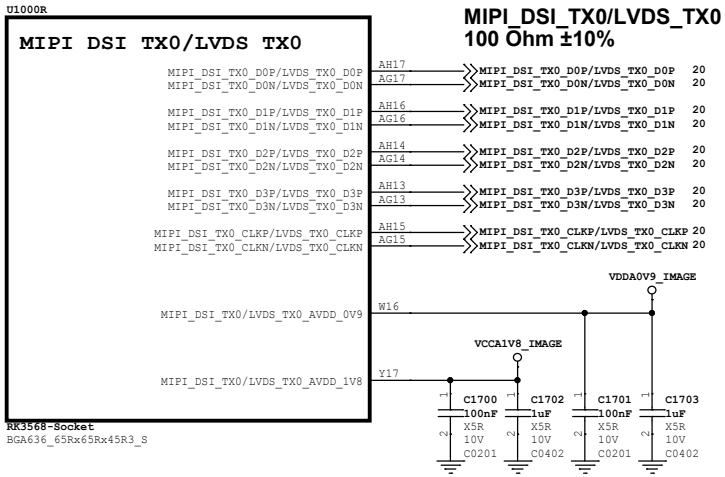
RK3568_M(VCCIO6 Domain)



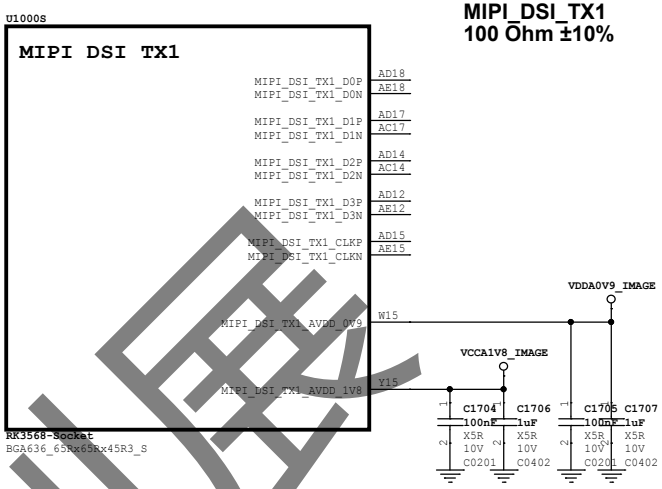
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	09.RK3568_VI Interface				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	9 of 17

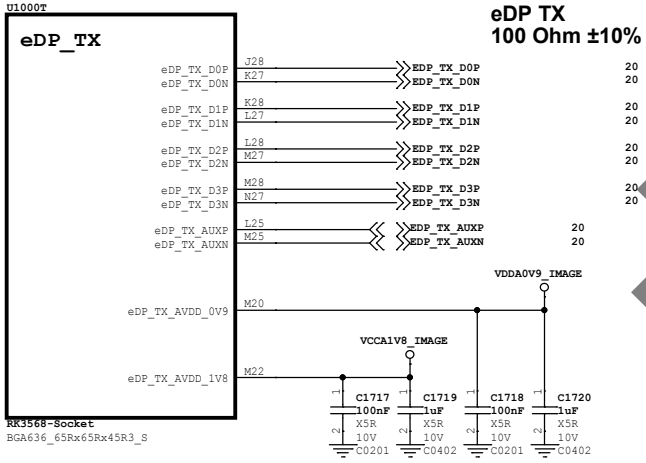
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



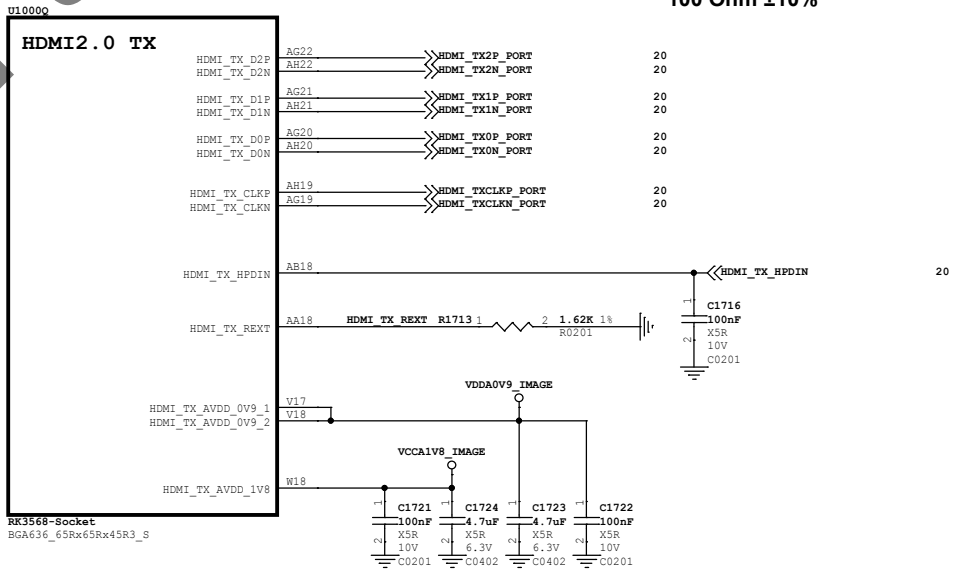
RK3568_S(MIPI_DSI_TX1)



RK3568_T(eDP TX)



RK3568_Q(HDMI2.0 TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	10.RK3568_VO Interface_1				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	10 of 17

RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

RK3568-Socket

BGA636_65Rx65Rx45R3_S

AG6 GMAC1_INT/PMEB_GPIO2_D0 20
AD7 GMAC1_RSTn_GPIO2_D1 20
AC8 GMAC0_INT/PMEB_GPIO2_D2 20
AC7 GMAC0_RSTn_GPIO2_D3 20
AF5
AF6
AD6
AH5

AH4 BT_REG_ON_H_GPIO3_A0 20

AB8 BT_WAKE_HOST_H_GPIO3_A1 20
AE5 HOST_WAKE_BT_H_GPIO3_A2 20
AG4 I2S3_SCLK_M0 20
AF4 I2S3_LRCK_M0 20
AH3 I2S3_SDO_M0 20
AG3 I2S3_SDI_M0 20
AH2 GMAC1_RXCLK_M0 20
AG2

for BT

AG1 UART4_RX_M1 20
AE4 UART4_TX_M1 20
AF1 I2C5_SCL_M0 20
AE1 I2C5_SDA_M0 20
AE2 GPIO3_B5 20
AE3 GPIO3_B6 20
AD4 UART3_TX_M1 20
AD2 UART3_RX_M1 20

AD1 GSENSOR_INT_L_GPIO3_C1 20
AA7 HP_DET_L_GPIO3_C2 20
AC4 GPIO3_C3 20

AC3 GPIO3_C4 20
AC2 SPDIF_TX_M1 20

VCC_3V3

V10 VCCIO5_1
V11 VCCIO5_2

C1800 100nF X5R 10V C0201

C1801 1uF X5R 6.3V C0402

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	11.RK3568_VO Interface_2				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	11 of 17

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u	D18
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u	E18
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/ GPIO1_A2_d	A19
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/ GPIO1_A3_d	B19
I2S1_SCLK_RX_M0	/ UART4_RX_M0 / PDM_CLK1_M0			/ SPDIF_TX_M0		/ GPIO1_A4_d	F18
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/ GPIO1_A5_d	A20
I2S1_LRCK_RX_M0	/ UART4_TX_M0 / PDM_CLK0_M0			/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d	C20
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d	B20
I2S1_SDO1_M0	/ I2S1_SDI3_M0 / PDM_SDI3_M0		/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/ GPIO1_B0_d	D20
I2S1_SDO2_M0	/ I2S1_SDI2_M0 / PDM_SDI2_M0		/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/ GPIO1_B1_d	E20
I2S1_SDO3_M0	/ I2S1_SDI1_M0 / PDM_SDI1_M0		/ PCIE20_PERSTn_M2			/ GPIO1_B2_d	A21
	I2S1_SDI0_M0 / PDM_SDI0_M0					/ GPIO1_B3_d	B21
						VCCIO1	H17

D18 — I2C3_SDA_M0 — 20
E18 — I2C3_SCL_M0 — 20
A19 — I2S1_MCLK_M0_RK809 — 21
B19 — I2S1_SCLK_TX_M0_RK809 — 21
F18
A20 — I2S1_LRCK_TX_M0_RK809 — 21
C20 — PDM_CLK0_M0_RK809 — 21
B20 — I2S1_SDO0_M0_RK809 — 21
D20
E20
A21
B21 — I2S1_SDI0_M0/PDM_SDI0_M0_RK809 — 21

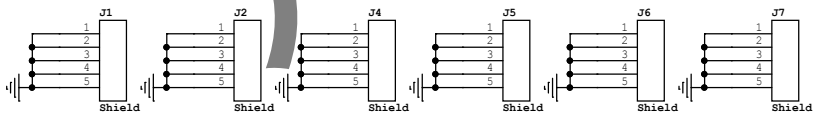
VCCIO_ACODEC

H17 — C1900 100nF X5R 10V C0201 — 1 / 2

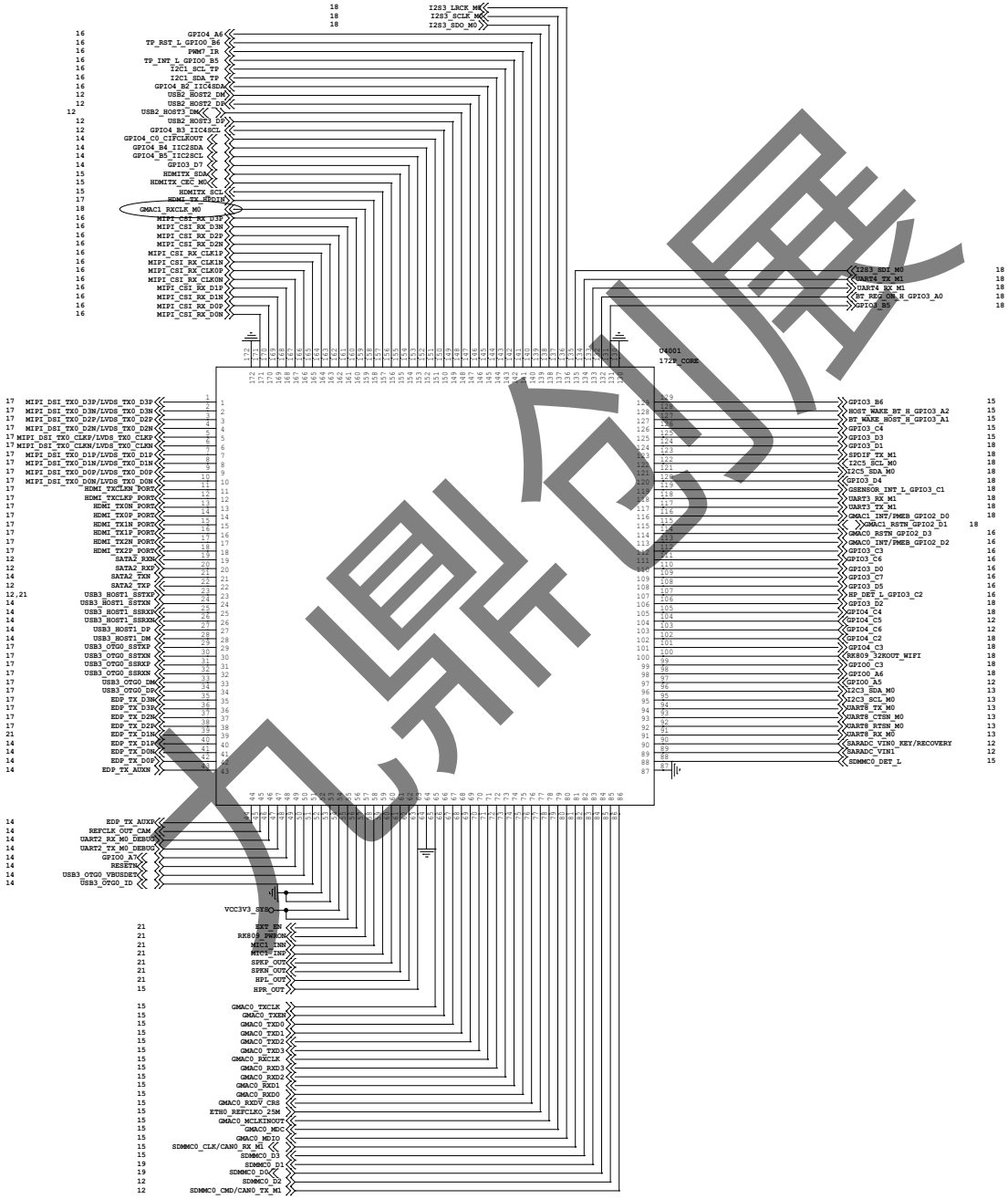
RK3568-Socket

BGA636_65Rx65Rx45R3_S

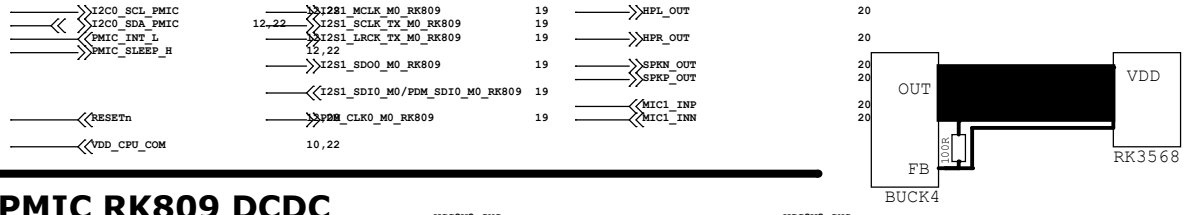
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	12.RK3568_Audio Interface				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	12 of 17



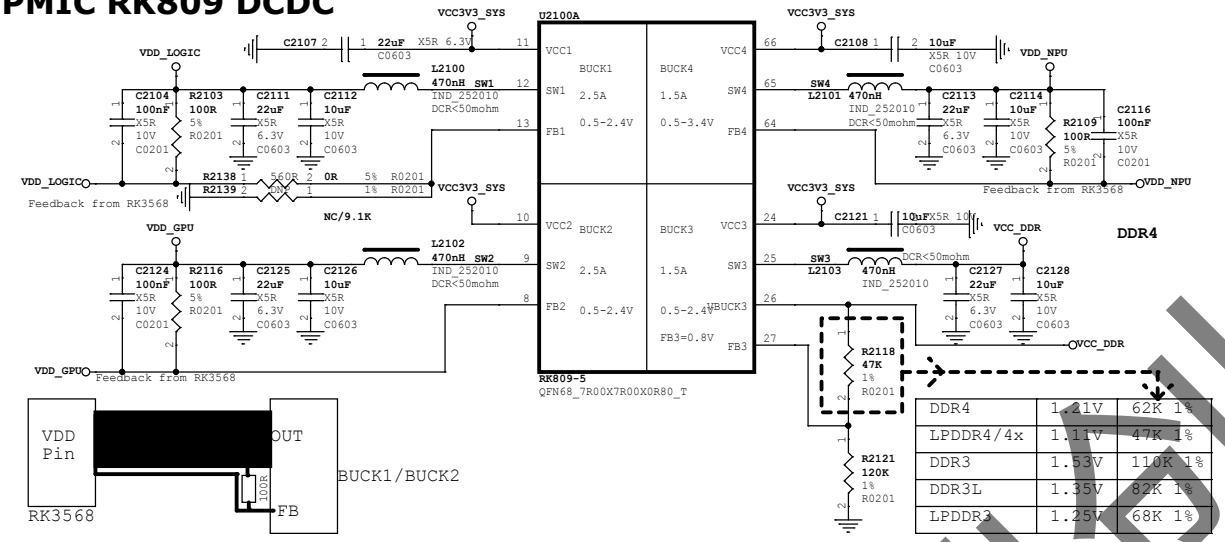
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	16.Connector				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	16 of 17



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	x3568cv1		
File:	17.172_CORE_CON		
Date:	Thursday, June 16, 2022	Rev:	V1.0
Designed by: Zhangdz	Reviewed by: Default	Sheet:	17 of 17

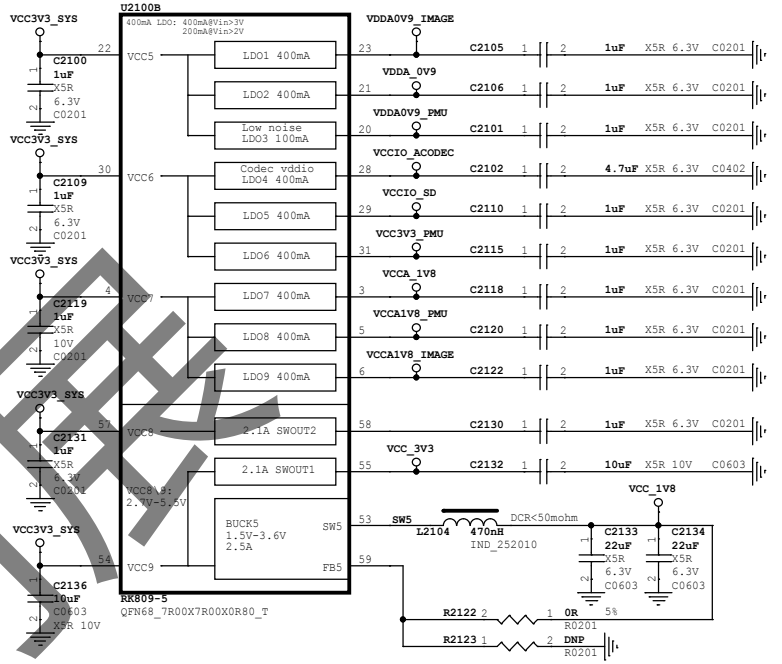


PMIC RK809 DCDC

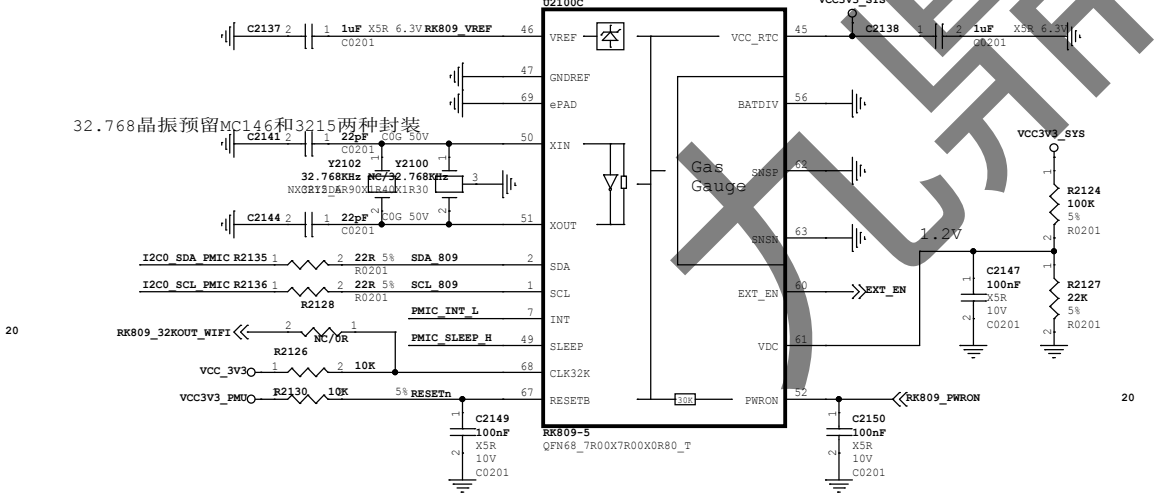


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

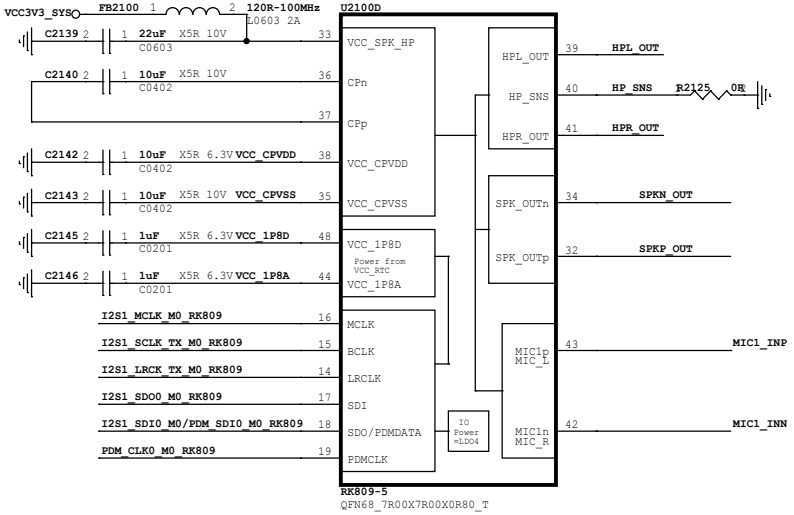
PMIC RK809 LDO



PMIC RK809 Managerment

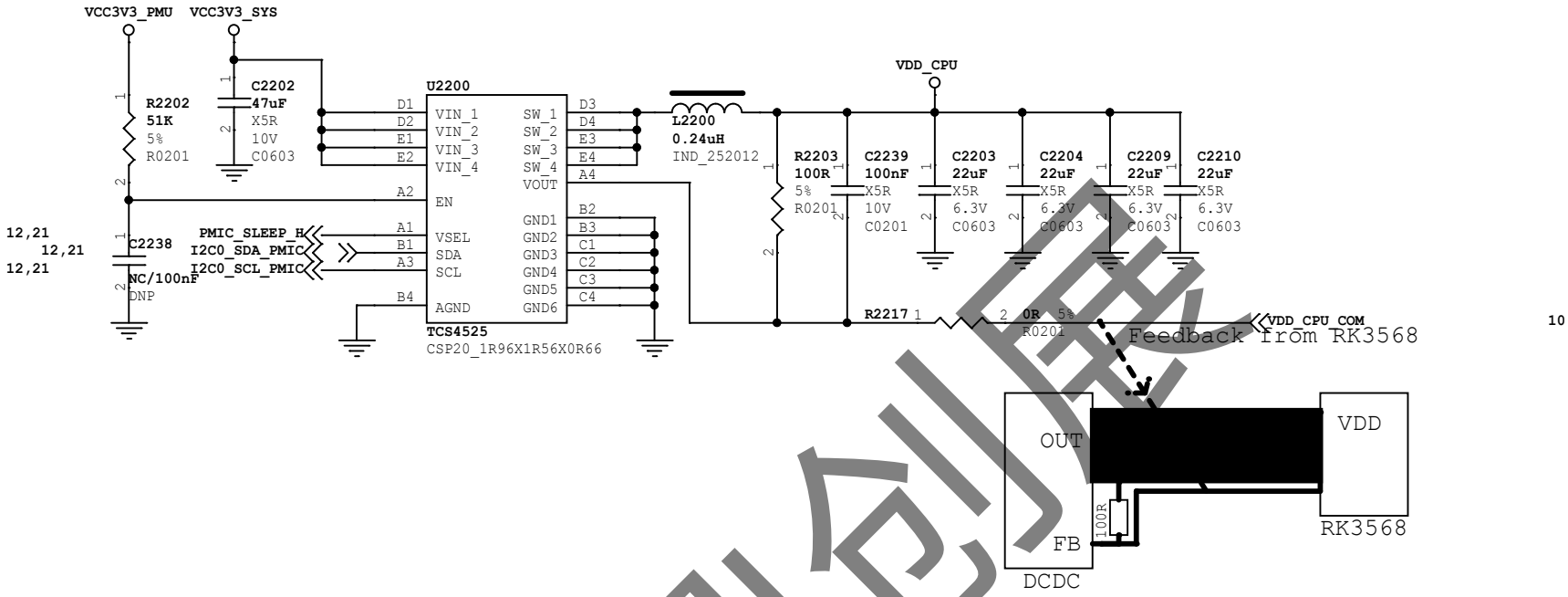


PMIC RK809 CODEC

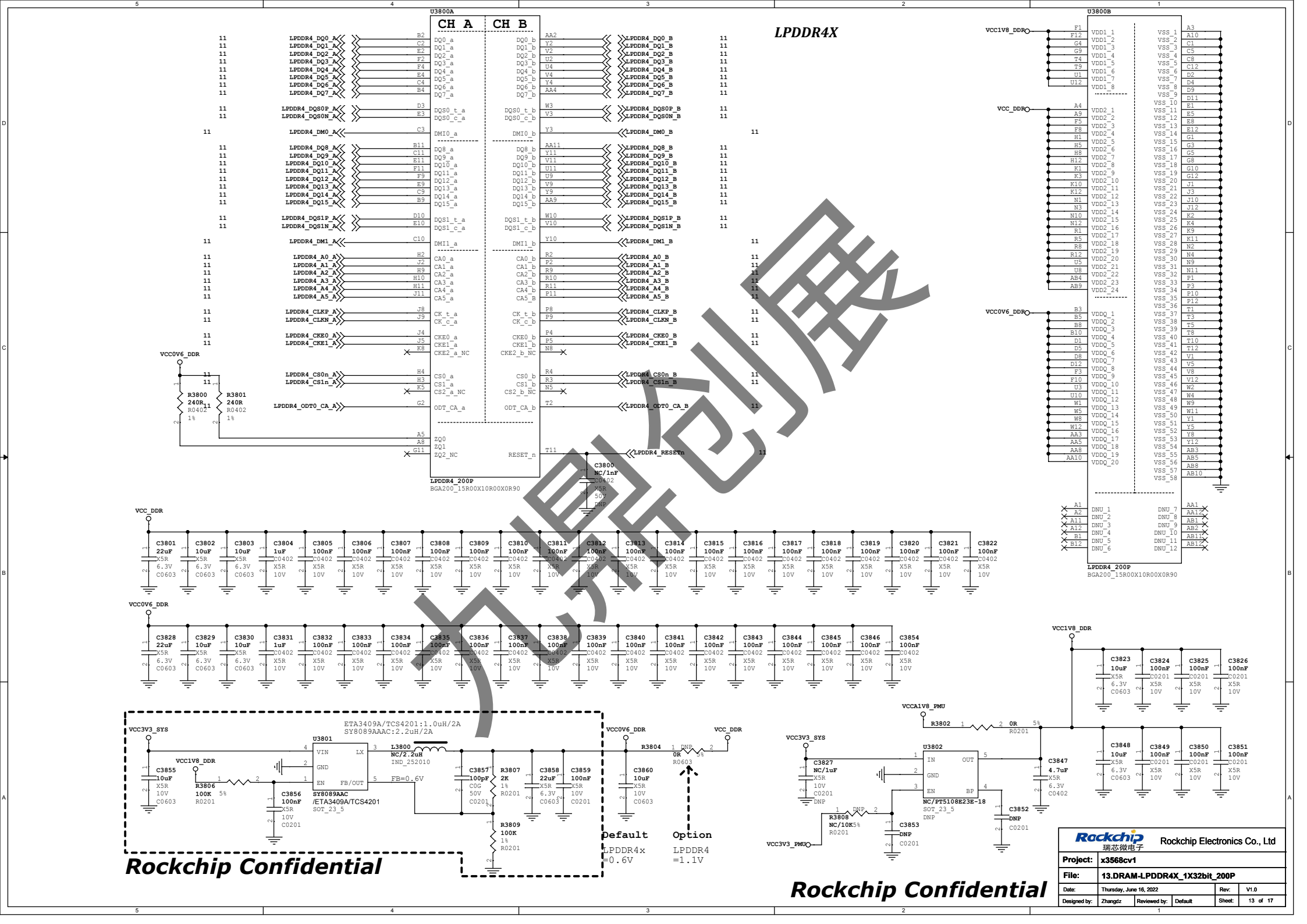


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	14.Power_PMIC				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	14 of 17

VDD_CPU



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	x3568cv1				
File:	15.Power_other				
Date:	Thursday, June 16, 2022			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	15 of 17


LPDDR4X
U3800A
CH A
CH B
LPDDR4_DQ0_A
LPDDR4_DQ1_A
LPDDR4_DQ2_A
LPDDR4_DQ3_A
LPDDR4_DQ4_A
LPDDR4_DQ5_A
LPDDR4_DQ6_A
LPDDR4_DQ7_A
LPDDR4_DQS0P_A
LPDDR4_DQS0N_A
LPDDR4_DM0_A
LPDDR4_DQ8_A
LPDDR4_DQ9_A
LPDDR4_DQ10_A
LPDDR4_DQ11_A
LPDDR4_DQ12_A
LPDDR4_DQ13_A
LPDDR4_DQ14_A
LPDDR4_DQ15_A
LPDDR4_DQS1P_A
LPDDR4_DQS1N_A
LPDDR4_DM1_A
LPDDR4_A0_A
LPDDR4_A1_A
LPDDR4_A2_A
LPDDR4_A3_A
LPDDR4_A4_A
LPDDR4_A5_A
LPDDR4_CLKP_A
LPDDR4_CLKN_A
LPDDR4_CKE0_A
LPDDR4_CKE1_A
LPDDR4_CS0n_A
LPDDR4_CS1n_A
LPDDR4_ODT0_CA_A
LPDDR4_DQ0_B
LPDDR4_DQ1_B
LPDDR4_DQ2_B
LPDDR4_DQ3_B
LPDDR4_DQ4_B
LPDDR4_DQ5_B
LPDDR4_DQ6_B
LPDDR4_DQ7_B
LPDDR4_DQS0P_B
LPDDR4_DQS0N_B
LPDDR4_DM0_B
LPDDR4_DQ8_B
LPDDR4_DQ9_B
LPDDR4_DQ10_B
LPDDR4_DQ11_B
LPDDR4_DQ12_B
LPDDR4_DQ13_B
LPDDR4_DQ14_B
LPDDR4_DQ15_B
LPDDR4_DQS1P_B
LPDDR4_DQS1N_B
LPDDR4_DM1_B
LPDDR4_A0_B
LPDDR4_A1_B
LPDDR4_A2_B
LPDDR4_A3_B
LPDDR4_A4_B
LPDDR4_A5_B
LPDDR4_CLKP_B
LPDDR4_CLKN_B
LPDDR4_CKE0_B
LPDDR4_CKE1_B
LPDDR4_CS0n_B
LPDDR4_CS1n_B
LPDDR4_ODT0_CA_B
LPDDR4_RESETn
LPDDR4_200P
BGA200_15R00X10R00X0R90
U3800B
VCC1V8_DDR
VCC_DDR
VCC0V6_DDR
R3800 240R R0402 1%
R3801 240R R0402 1%
C3800 NC/1nF C0402 X5R 50V DNP
C3801 22uF X5R 6.3V C0603
C3802 10uF X5R 6.3V C0603
C3803 10uF X5R 6.3V C0603
C3804 1uF C0402 X5R 10V
C3805 100nF C0402 X5R 10V
C3806 100nF C0402 X5R 10V
C3807 100nF C0402 X5R 10V
C3808 100nF C0402 X5R 10V
C3809 100nF C0402 X5R 10V
C3810 100nF C0402 X5R 10V
C3811 100nF C0402 X5R 10V
C3812 100nF C0402 X5R 10V
C3813 100nF C0402 X5R 10V
C3814 100nF C0402 X5R 10V
C3815 100nF C0402 X5R 10V
C3816 100nF C0402 X5R 10V
C3817 100nF C0402 X5R 10V
C3818 100nF C0402 X5R 10V
C3819 100nF C0402 X5R 10V
C3820 100nF C0402 X5R 10V
C3821 100nF C0402 X5R 10V
C3822 100nF C0402 X5R 10V
C3828 22uF X5R 6.3V C0603
C3829 10uF X5R 6.3V C0603
C3830 10uF X5R 6.3V C0603
C3831 1uF C0402 X5R 10V
C3832 100nF C0402 X5R 10V
C3833 100nF C0402 X5R 10V
C3834 100nF C0402 X5R 10V
C3835 100nF C0402 X5R 10V
C3836 100nF C0402 X5R 10V
C3837 100nF C0402 X5R 10V
C3838 100nF C0402 X5R 10V
C3839 100nF C0402 X5R 10V
C3840 100nF C0402 X5R 10V
C3841 100nF C0402 X5R 10V
C3842 100nF C0402 X5R 10V
C3843 100nF C0402 X5R 10V
C3844 100nF C0402 X5R 10V
C3845 100nF C0402 X5R 10V
C3846 100nF C0402 X5R 10V
C3854 100nF C0402 X5R 10V
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
U3801
VIN
GND
EN
FB/OUT
LX
SY8089AAC
/ETA3409A/TCS4201
SOT_23_5
L3800 NC/2.2uH IND_252010
FB=0.6V
R3806 100K 5% R0201
C3855 10uF X5R 10V C0603
C3856 100nF X5R 10V C0201
C3857 100pF C0G 50V C0201
R3807 2K 1% R0201
C3858 22uF X5R 6.3V C0603
C3859 100nF X5R 10V C0201
R3809 100K 1% R0201
R3804 DNP 0R 5% R0603
C3860 10uF X5R 10V C0603
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
VCCA1V8_PMU
R3802 0R 5% R0201
U3802
IN
GND
EN
OUT
BP
NC/PT5108E23E-18
SOT_23_5
DNP
C3827 NC/1uF X5R 10V C0201 DNP
C3847 4.7uF X5R 6.3V C0402
C3852 DNP C0201
C3853 DNP C0201
R3808 NC/10K 5% R0201
VCC3V3_PMU
C3823 10uF X5R 6.3V C0603
C3824 100nF C0201 X5R 10V
C3825 100nF C0201 X5R 10V
C3826 100nF C0201 X5R 10V
C3848 10uF X5R 6.3V C0603
C3849 100nF C0201 X5R 10V
C3850 100nF C0201 X5R 10V
C3851 100nF C0201 X5R 10V
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瑞芯微电子
Project: x3568cv1
File: 13.DRAM-LPDDR4X_1X32bit_200P
Date: Thursday, June 16, 2022
Rev: V1.0
Designed by: Zhangdz
Reviewed by: Default
Sheet: 13 of 17